Service Guide

Publication number 01670-97006
First edition, October 1996

For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

HP 1670D-Series Logic Analyzers

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The HP 1670D-Series are 100-MHz State/250-MHz Timing Logic Analyzers.

Features

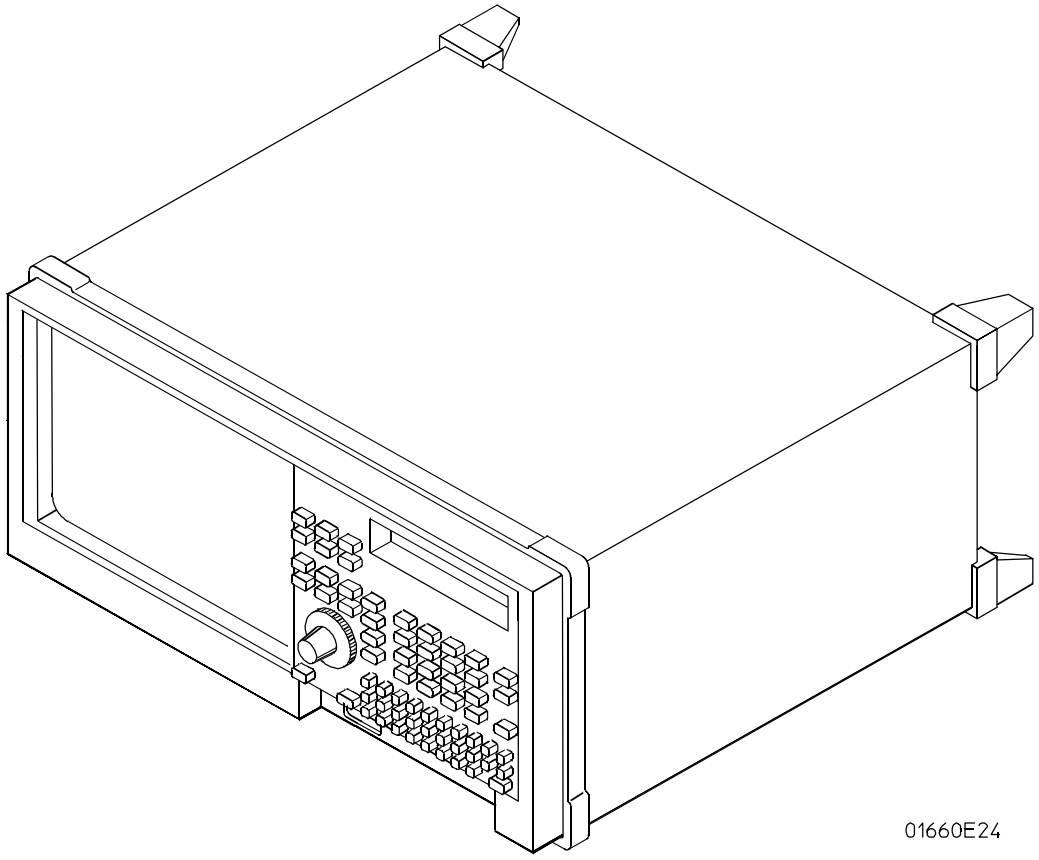
Some of the main features of the HP 1670D-Series Logic Analyzers are as follows:

- 132 data channels and 4 clock/data channels in the HP 1670D
- 98 data channels and 4 clock/data channels in the HP 1671D
- 64 data channels and 4 clock/data channels in the HP 1672D
- 3.5-inch flexible disk drive
- 540-MB hard disk drive
- HP-IB, RS-232-C, Centronics, and LAN interfaces
- Thinlan and Ethertwist LAN ports
- Variable setup/hold time
- 64 K memory on all channels, 128 K in half-channel mode
- 1.0 M memory on all channels available as an option (2.0 M memory in half-channel mode)
- Marker measurements
- 12 levels of trigger sequencing for state and 10 levels of sequential triggering for timing
- Full programmability
- DIN mouse
- DIN keyboard support

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the HP 1670D-series logic analyzers.

This logic analyzer can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.



HP 1670D-Series Logic Analyzer

In This Book

This book is the service guide for the HP 1670D-Series Logic Analyzers and is divided into eight chapters.

Chapter 1 contains information about the logic analyzer and includes accessories, specifications and characteristics, and equipment required for servicing.

Chapter 2 tells how to prepare the logic analyzer for use.

Chapter 3 gives instructions on how to test the performance of the logic analyzer.

Chapter 4 contains calibration instructions for the logic analyzer.

Chapter 5 contains self-tests and flowcharts for troubleshooting the logic analyzer.

Chapter 6 tells how to replace assemblies of the logic analyzer and how to return them to Hewlett-Packard.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the logic analyzer works and what the self-tests are checking.

Contents

1

General Information

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the HP 1670D-series logic analyzers. The part numbers are current as of the print date of this edition of the Service Guide, but further upgrades may change the part numbers. Do not be concerned if the accessories you receive have different part numbers.

Accessories Supplied	HP Part Number	Qty
Probe tip assemblies	01650-61608	Note 1
Probe cables	01660-61605	Note 2
Grabbers (20 per pack)	5090-4356	Note 1
Probe ground (5 per pack)	5959-9334	Note 1
Double Probe Adapter	16542-61607	1
User's Guide	01670-99004	1
Accessories Pouch	01660-84501	1
RS-232-C Loopback Connector	01650-63202	1
PS2 Mouse	A2839B	1

Note 1 Quantities: 8 - 1670D
6 - 1671D
4 - 1672D

Note 2 Quantities: 4 - 1670D
3 - 1671D
2 - 1672D

Accessories Available

Other accessories available for the HP 1670D-series logic analyzer are listed in the *Accessories for HP Logic Analyzers* brochure.

Specifications

The specifications are the performance standards against which the product is tested.

Maximum State Speed (selectable)	100 MHz
Minimum Master to Master Clock Time*	10.0 ns
Minimum State Clock Pulse Width*	3.5 ns
Threshold Accuracy	± (100 mV + 3% of threshold setting)

Setup/Hold Time:*

Single Clock, Single Edge	0.0/3.5 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal VH = –0.9 V, VL = –1.7 V, slew rate = 1 V/ns, and threshold = –1.3 V.

Characteristics

These characteristics are not specifications, but are included as additional information.

		Full Channel	**Half Channel**
Maximum State Clock Rate		100 MHz	not applicable
Maximum Conventional Timing Rate		125 MHz	250 MHz
Memory Depth		64K*	128K*
Channel Count:			
	HP 1670D	136	68
	HP 1671D	102	51
	HP 1672D	68	34

* Option 030 provides 1024K/2048K memory depth in full/half-channel modes.

Supplemental Characteristics

Probes

Input Resistance	100 kΩ, ± 2%
Input Capacitance	~ 8 pF
Minimum Voltage Swing	500 mV, peak-to-peak, CAT I
Threshold Range	± 6.0 V, adjustable in 50-mV increments, CAT I

State Analysis

State/Clock Qualifiers	4
Time Tag Resolution*	8 ns or 0.1%, whichever is greater
Maximum Time Count Between States	34 seconds
Maximum State Tag Count*	4.29×10^9

Timing Analysis

Sample Period Accuracy	0.01 % of sample period
Channel-to-Channel Skew	2 ns, typical
Minimum Glitch Width	3.5 ns
Time Interval Accuracy	± [sample period + channel-to-channel skew +(0.01%)(time reading)]

Triggering

Sequencer Speed	125 MHz, maximum
State Sequence Levels	12
Timing Sequence Levels	10
Maximum Occurrence Counter Value	1,048,575
Pattern Recognizers	10
Maximum Pattern Width	136 channels in HP 1670D, 102 channels in HP 1671D, 68 channels in HP 1672D
Range Recognizers	2
Range Width	32 bits each
Timers	2
Timer Value Range	400 ns to 500 seconds
Glitch/Edge Recognizers	2 (timing only)
Maximum Glitch/Edge Width	136 channels in HP 1670D, 102 channels in HP 1671D, 68 channels in HP 1672D

*Maximum state clock rate with time or state tags on is 100 MHz. When all pods are assigned to a state or timing machine, time or state tags halve the memory depth.

Measurement and Display Functions

Displayed Waveforms 24 lines maximum, with scrolling across 96 waveforms.

Measurement Functions

Run/Stop Functions Run starts acquisition of data in specified trace mode.

Stop Stop halts acquisition and displays the current acquisition data.

Trace Mode Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until Stop is pressed or until the time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range.

Indicators

Activity Indicators Provided in the Configuration and Format menus for identifying high, low, or changing states on the inputs.

Markers Two markers (X and O) are shown as vertical dashed lines on the display.

Trigger Displayed as a vertical dashed line in the Timing Waveform display and as line 0 in the State Listing display.

Data Entry/Display

Labels Channels may be grouped together and given a 6-character name. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label.

Display Modes State listing, State Waveforms, Chart, Compare Listing, Compare Difference Listing, Timing Waveforms, and Timing Listings. State Listing and Timing Waveforms can be time-correlated on the same displays.

Timing Waveform Pattern readout of timing waveforms at X or O marker.

Bases Binary, Octal, Decimal, Hexadecimal, ASCII (display only), Two's Complement, and Symbols.

Symbols 1,000 maximum. Symbols can be downloaded over Ethernet LAN, RS-232-C, or HP-IB connection.

Marker Functions

Time Interval The X and O markers measure the time interval between a point on a timing waveform and the trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (state analyzer only) The X and O markers measure the number of tagged states between one state and trigger or between two states.

Patterns The X and O markers can be used to locate the nth occurrence of a specified pattern from trigger, or from the beginning of data. The O marker can also find the nth occurrence of a pattern from the X marker.

Statistics X and O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

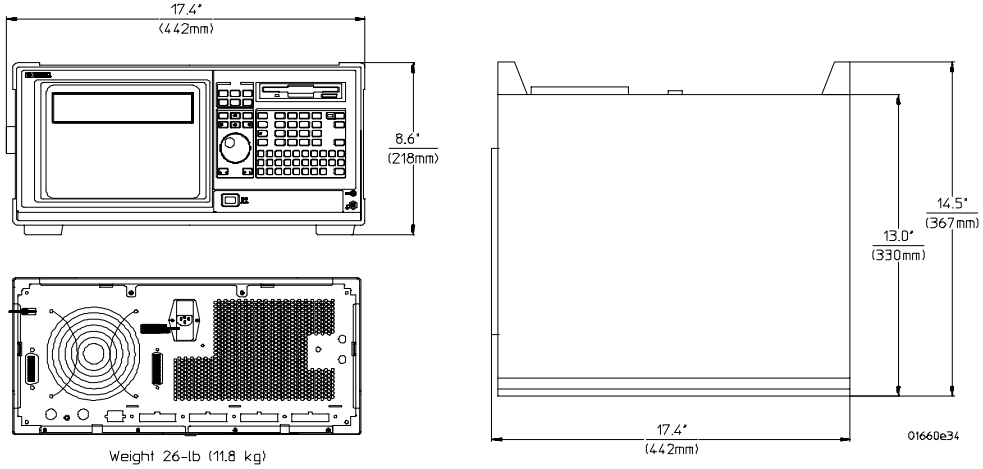
Auxiliary Power

Power Through Cables	1/3 amp at 5 V maximum per cable, CAT 1

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F). Disk media, 10 °C to 40 °C (+50 °F to 104 °F).
Humidity	Instrument, probe lead sets, and cables, up to 80% relative humidity at +40 °C (+122 °F).
Altitude	To 3067 m (10,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Dimensions



Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8131A Option 020	P,T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A mainframe with HP 54751A plugin module	P
Function Generator	Accuracy ≤ $(5)(10^{-6})$ × frequency, DC offset voltage ±6.3 V	HP 3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A	P
BNC-Banana Cable		HP 11001-60001	P
BNC Tee	BNC (m)(f)(f)	HP 1250-0781	P
Cable	BNC (m)(m) 48 inch	HP 10503A	P,T
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	HP 1250-1200	P, T
Adapter	SMA(f)-BNC(m)	HP 1250-2015	P
Coupler (Qty 4)	BNC (m)(m)	HP 1250-0216	P, T
20:1 Probes (Qty 2)		HP 54006A	P
BNC Coax Cable	BNC(m)(m), >2 GHz bandwidth, >1 meter length	HP 10503A	T
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P,T
Digitizing Oscilloscope	> 100 MHz Bandwidth	HP 54600B	T
BNC Shorting Cap		HP 1250-0074	T
BNC-Banana Adapter		HP 1251-2277	T
Light Power Meter		United Detector 351	A
Alignment Tool		HP 8710-1300	A

*A = Adjustment P = Performance Tests T = Troubleshooting
**Instructions for making these test connectors are in chapter 3, "Testing Performance."

2

Preparing for Use

Preparing For Use

This chapter gives you instructions for preparing the logic analyzer for use.

Power Requirements

The logic analyzer requires a power source of either 115 Vac or 230 Vac, –22 % to +10 %, single phase, 48 to 66 Hz, 200 Watts maximum power.

Operating Environment

The operating environment is listed in chapter 1. The logic analyzer will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the logic analyzer within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Note the recommended noncondensing humidity. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to +75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the logic analyzer from temperature extremes which cause condensation on the instrument.

To inspect the logic analyzer

1. **Inspect the shipping container for damage.**

   If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2. **Check the supplied accessories.**

   Accessories supplied with the logic analyzer are listed in "Accessories" in chapter 1.

3. **Inspect the product for physical damage.**

   Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Hewlett-Packard Sales Office. Arrangements for repair or replacement are made, at Hewlett-Packard's option, without waiting for a claim settlement.

To apply power

1. Check that the line voltage selector, located on the rear panel, is on the correct setting and the correct fuse is installed.
   See also, "To set the line voltage" on this page.
2. Connect the power cord to the instrument and to the power source.
   This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to chapter 7, "Replaceable Parts," for option numbers of available power cables and plug configurations.
3. Turn on the instrument power switch located on the front panel.

To operate the user interface

To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. For more information about the logic analyzer interface, refer to the *HP 1670D-Series Logic Analyzers User's Guide*.

To set the HP-IB address or to configure for RS-232-C, refer to the *HP 1670D-Series Logic Analyzer User's Guide*.

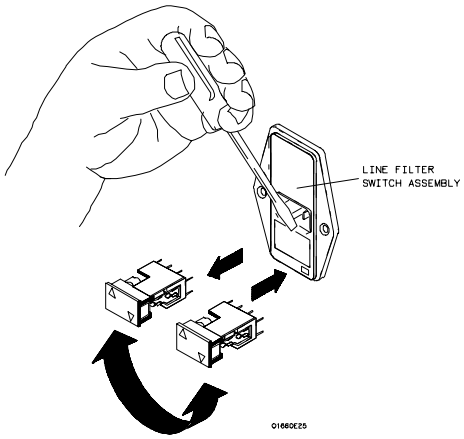
To set the line voltage

When shipped from HP, the line voltage selector is set and an appropriate fuse is installed for operating the instrument in the country of destination. To operate the instrument from a power source other than the one set, perform the following steps.

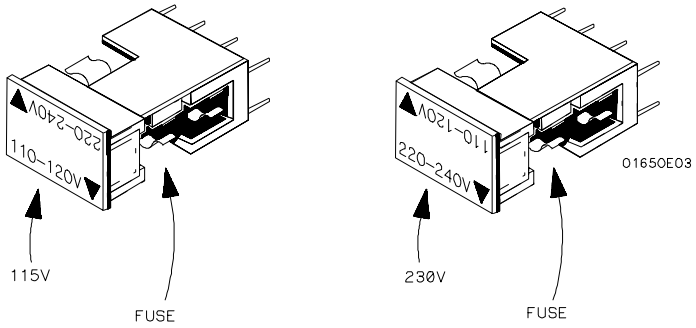
CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to the logic analyzer.

1. Turn the power switch to the Off position, then remove the power cord from the instrument.
2. Remove the fuse module by carefully prying at the top center of the fuse module until you can grasp it and pull it out by hand.



3 Reinsert the fuse module with the arrow for the appropriate line voltage aligned with the arrow on the line filter assembly switch.



4 Reconnect the power cord. Turn on the instrument by setting the power switch to the On position.

To degauss the display

If the logic analyzer has been subjected to strong magnetic fields, the CRT might become magnetized and display data might become distorted. To correct this condition, degauss the CRT with a conventional external television type degaussing coil.

To clean the logic analyzer

With the instrument turned off and unplugged, use mild soap and water to clean the front and cabinet of the logic analyzer. Harsh soap might damage the water-base paint.

To test the logic analyzer

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the logic analyzer does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

Testing Performance

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, you perform software tests (self-tests) and manual performance tests on the analyzer. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

The Logic Analyzer Interface

To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. For more information about the logic analyzer interface, refer to the *HP 1670D-Series Logic Analyzers User's Guide*.

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test. The examples in this chapter were performed using an HP 1670D. Other analyzers in the series will have appropriate pods showing on the screen.

The performance verification procedures starting on page 3–8 are each shown from power-up. To exactly duplicate the setups in the tests, save the power-up configuration to a file on a disk, then load that file at the start of each test.

If a test fails, check the test equipment setup, check the connections, and verify adequate grounding. If a test still fails, the most probable cause of failure would be the acquisition board.

Test Interval

Test the performance of the logic analyzer against specifications at two-year intervals.

Performance Test Record

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the logic analyzer over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number. Before testing the performance of the logic analyzer, warm-up the instrument and the test equipment for 30 minutes.

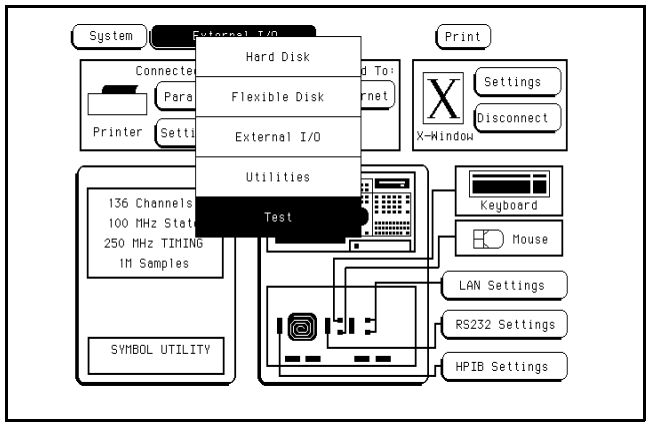
To perform the self-tests

The self-tests verify the correct operation of the logic analyzer. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analyzer, run the self-tests all at once.

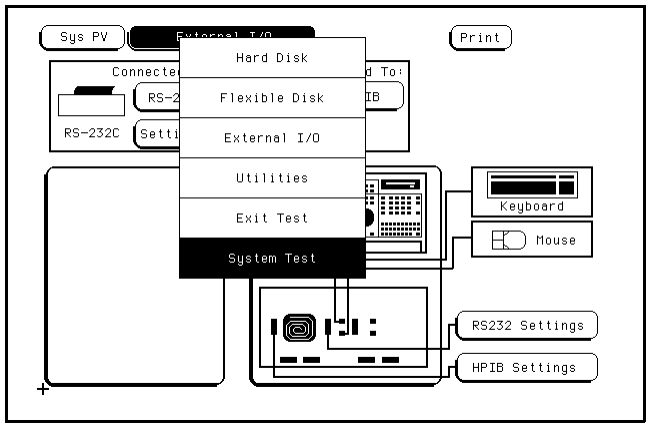
The performance verification (PV) self-tests consist of system PV tests and analyzer PV tests.

These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

1. Disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.
2. Press the System key. Select External I/O, then select Test in the pop-up menu.



3. Select the box labeled Load Test System.
4. Select the Analy PV field. then select SysPV in the pop-up menu. Select the field next to Sys PV, then select System Test in the pop-up menu.

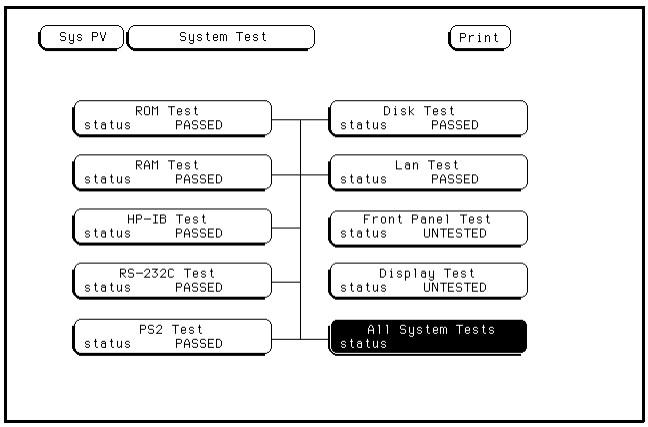


5 Install a formatted disk that is not write protected into the disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port.

6 Select All System Tests.

You can run all tests at one time, except for the Front Panel Test and Display Test, by running All System Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All System Tests changes from UNTESTED to TESTED. Note that the Front Panel Test and Display Test remain UNTESTED.



7 Select the Front Panel Test.

A screen duplicating the front panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color. Test the knob by turning it in both directions.

b Note any failures, then press the Done key a second time to exit the Front Panel Test. The status of the test changes from UNTESTED to TESTED.

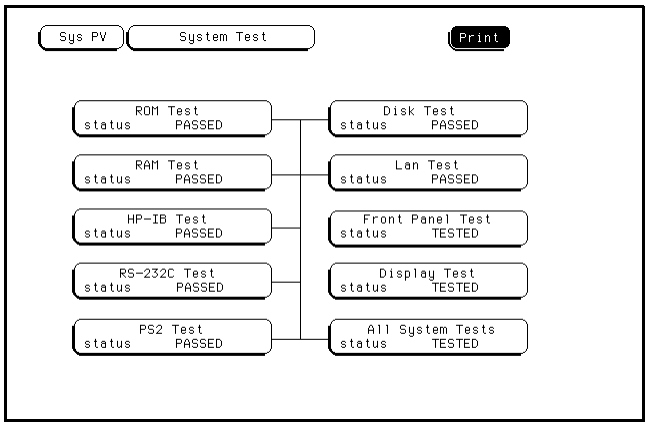
8 Select the Display Test.

A white grid pattern is displayed. These display screens are not normally used, but can be used to adjust the display. Refer to chapter 4, "Calibrating and Adjusting" for display adjustments.

a Select Continue and the screen changes to full bright.

b Select Continue and the screen changes to half bright.

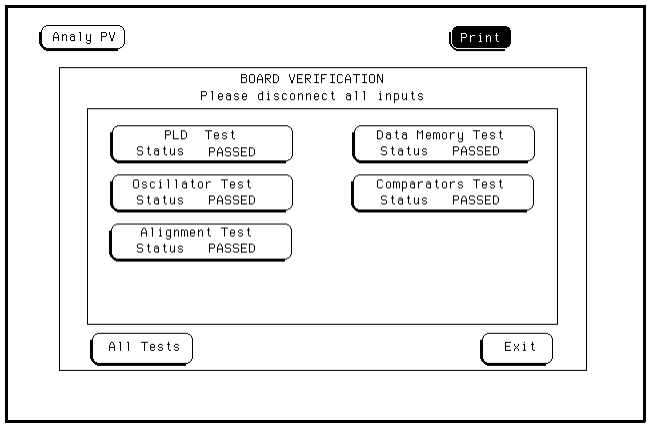
c Select Continue and the test screen shows the Display Test status changed to TESTED.



9 Select Sys PV, then select Analy PV in the pop-up menu. In the Analy PV menu, select Board Verification. In the Board Verification menu, select All Tests.

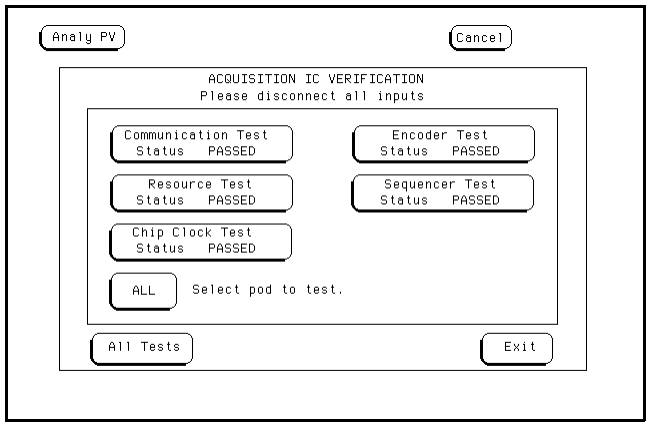
You can run all tests at one time by selecting All Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All Tests changes from UNTESTED to TESTED.



10 Select Exit to exit the Board Verification. In the Analy PV menu, select Acquisition IC Verification. In the Acquisition IC Verification menu, select All Tests.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All Tests changes from UNTESTED to TESTED.



11 Record the results of the tests on the performance test record at the end of this chapter.

12 To exit the test system, press the System key, then press the Select key. Select Exit Test, then select Exit Test System.

To make the test connectors

The test connectors connect the logic analyzer to the test equipment.

Materials Required

Description	Recommended Part	Qty
BNC (f) Connector	HP 1250-1032	5
100 Ω 1% resistor	HP 0698-7212	8
Berg Strip, 17-by-2		1
Berg Strip, 6-by-2		4
20:1 Probe	HP 54006A	2
Jumper wire		

1 Build four test connectors using BNC connectors and 6-by-2 sections of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

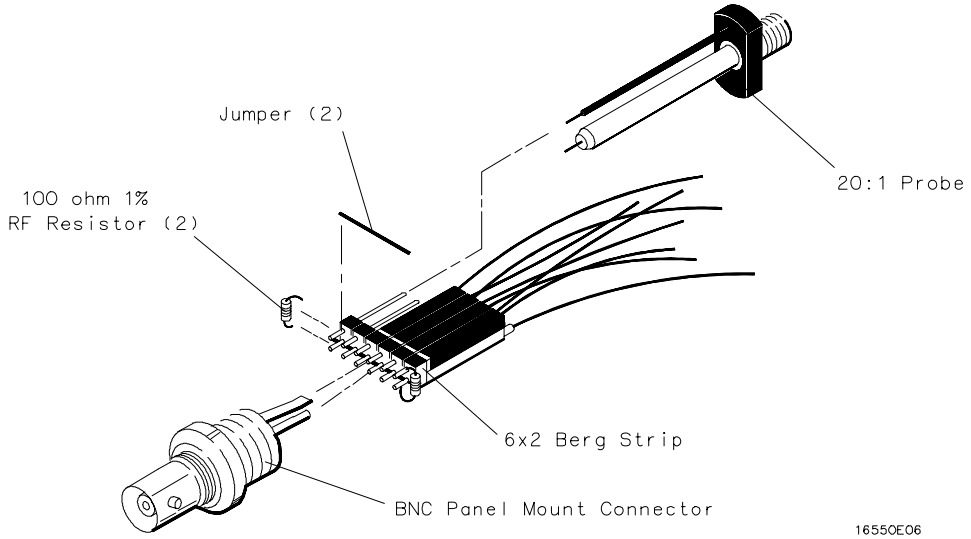
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



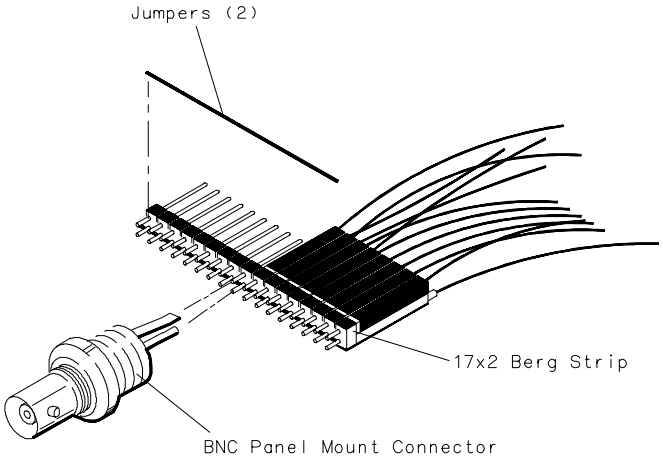
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



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To test the threshold accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy.

These instructions include detailed steps for testing the threshold settings of pod 1. After testing pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for pod 1, substituting the next pod for pod 1 in the instructions.

Each threshold test tells you to record the voltage reading in the performance test record located at the end of this chapter. To check if each test passed, verify that the voltage reading you record is within the limits listed on the performance test record.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A
Function Generator	Accuracy ≤ (5)(10^{-6}) × frequency, DC offset voltage ±6.3 V	HP 3325B Option 002
BNC-Banana Cable		HP 11001-60001
BNC Tee		HP 1250-0781
BNC Cable		HP 10503A
BNC Test Connector, 17x2		

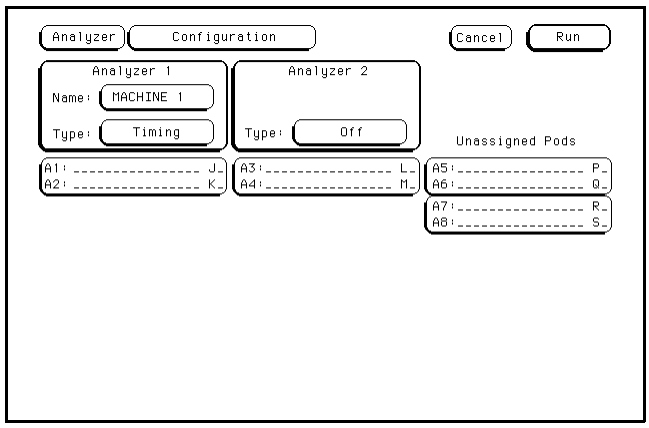
Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test.
2. Set up the function generator.
   - **a** Set up the function generator to provide a DC offset voltage at the Main Signal output.
   - **b** Disable any AC voltage to the function generator output, and enable the high voltage output.
   - **c** Monitor the function generator DC output voltage with the multimeter.

Set up the logic analyzer

1 Press the Config key.

2 Unassign Pods 3 and 4, Pods 5 and 6, and Pods 7 and 8. To unassign the pods, select the pod field. In the pop-up menu, select Unassigned.

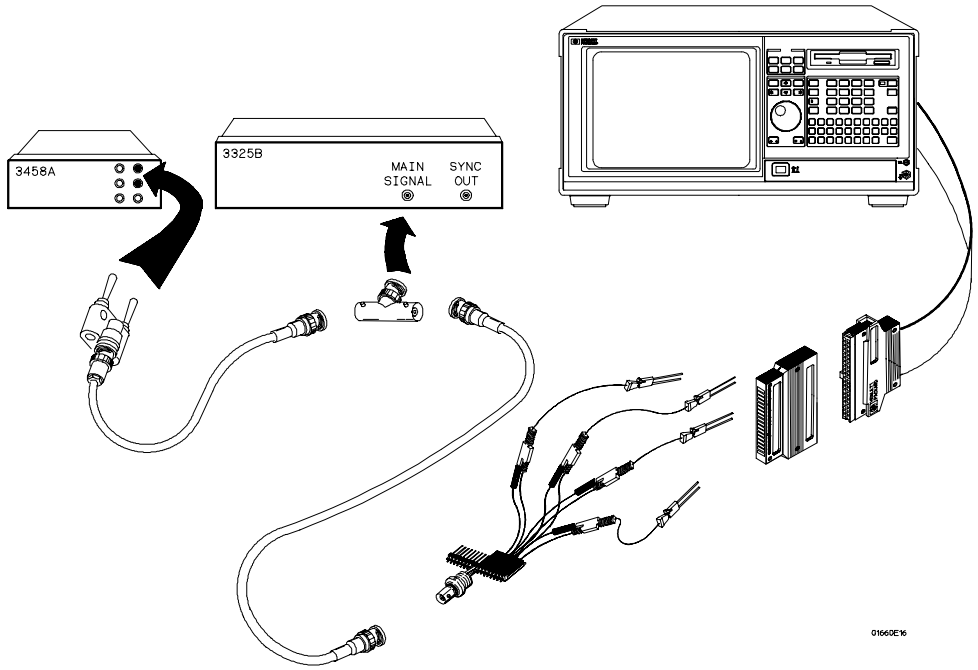


Connect the logic analyzer

1 Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of pod 1 to one side of the BNC Tee.

2 Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.

3 Connect the BNC Tee to the Main Signal output of the function generator.

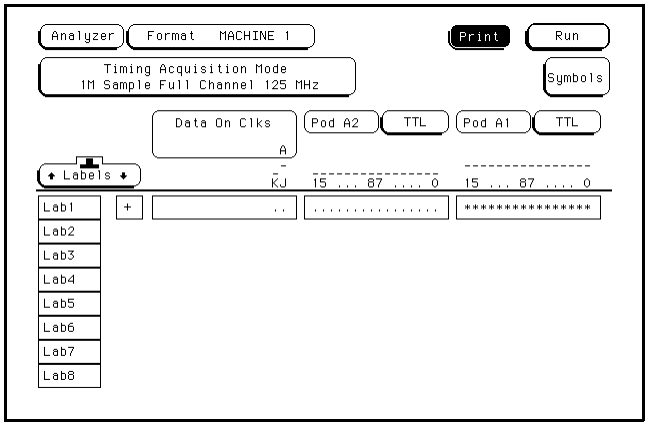


Test the TTL threshold

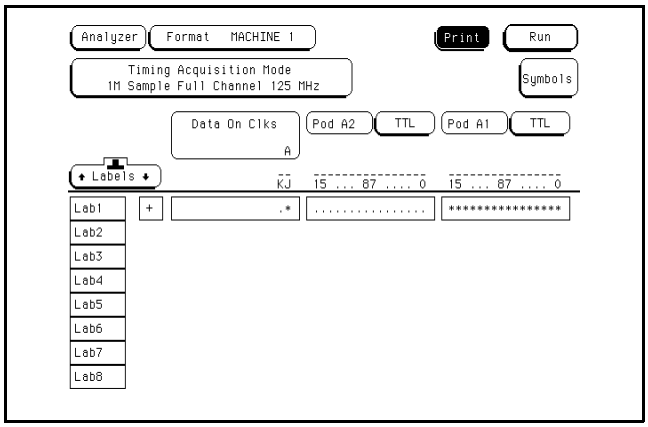
1 Press the Format key. Select the field to the right of Pod A1, then select TTL in the pop-up menu.

2 On the function generator front panel, enter 1.750 V ±1 mV DC offset. Use the multimeter to verify the voltage.

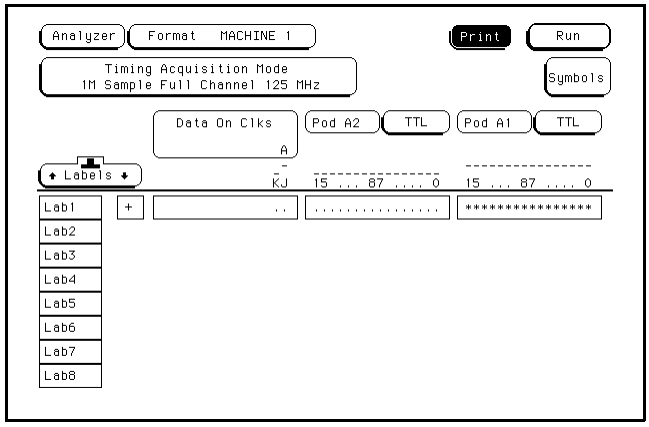
The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.



3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



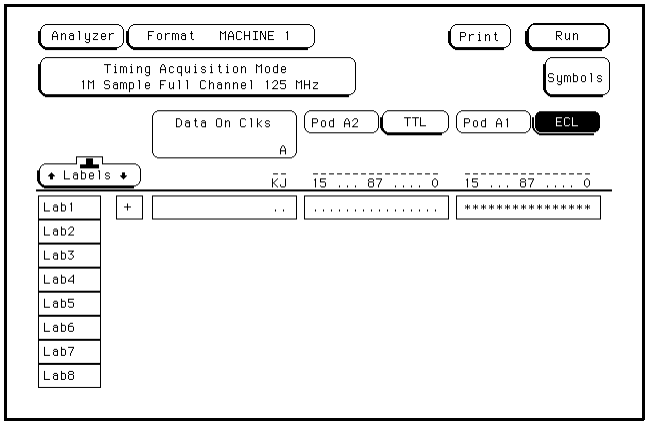
4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



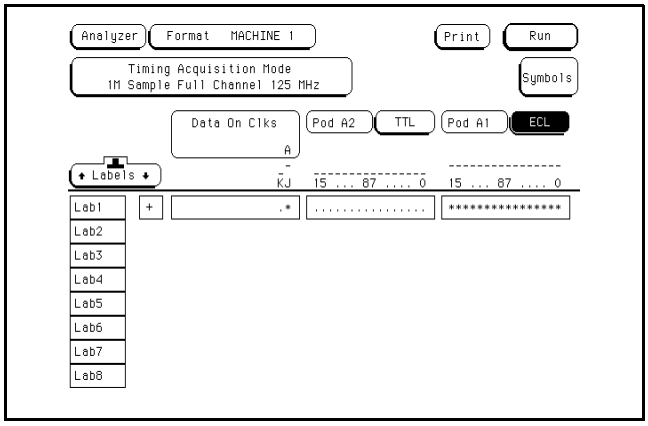
Test the ECL threshold

1. Select the field to the right of Pod A1, then select ECL in the pop-up menu.
2. On the function generator front panel, enter –1.160 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels are at a logic low. Record the function generator voltage in the performance test record.



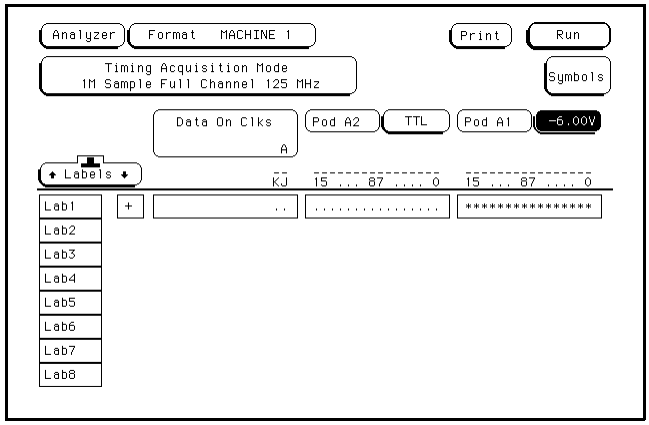
4. Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels are at a logic high. Record the function generator voltage in the performance test record.



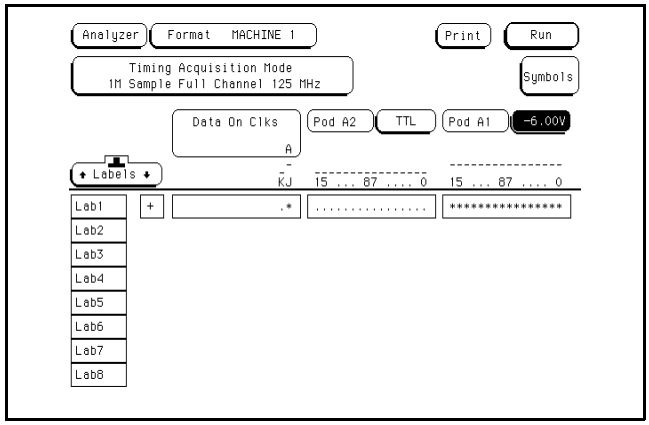
Test the – User threshold

1. Move the cursor to the field to the right of Pod A1. Type –6.00, then use the left and right cursor control keys to highlight V. Press the Select key.
2. On the function generator front panel, enter –5.718 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4. Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators show the channels at a logic high. Record the function generator voltage in the performance test record.



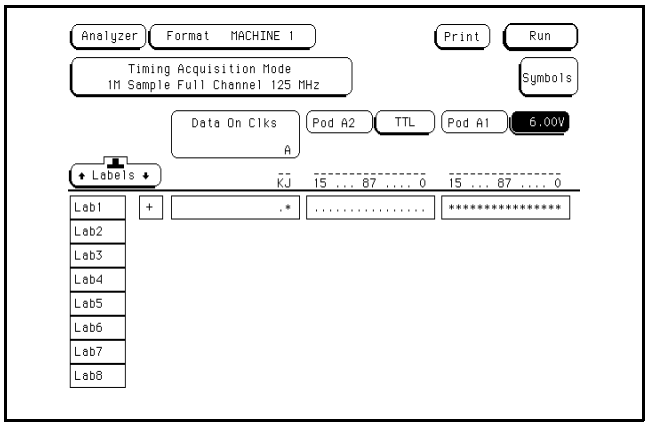
Test the + User threshold

1 Move the cursor to the field to the right of Pod A1. Type +6.00, then use the left and right cursor control keys to highlight V. Press the Select key.

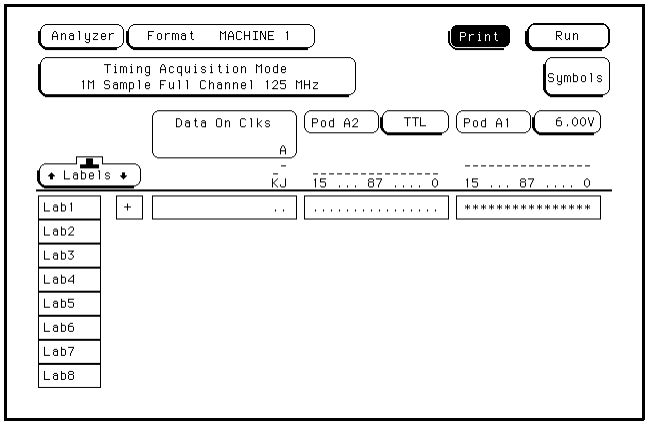
2 On the function generator front panel, enter +6.282 V ±1 mV DC offset. Use the multimeter to verify the voltage.

The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



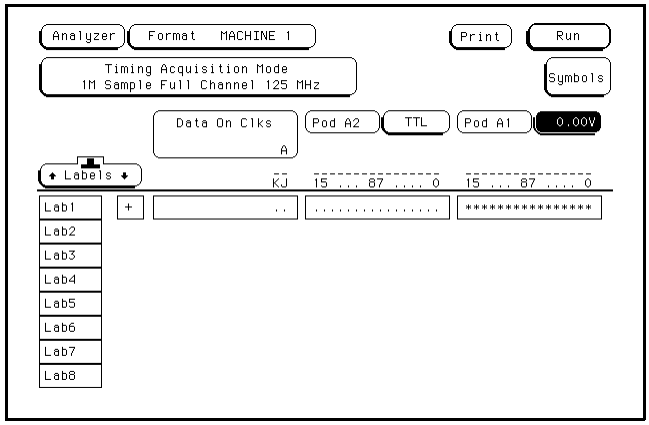
4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



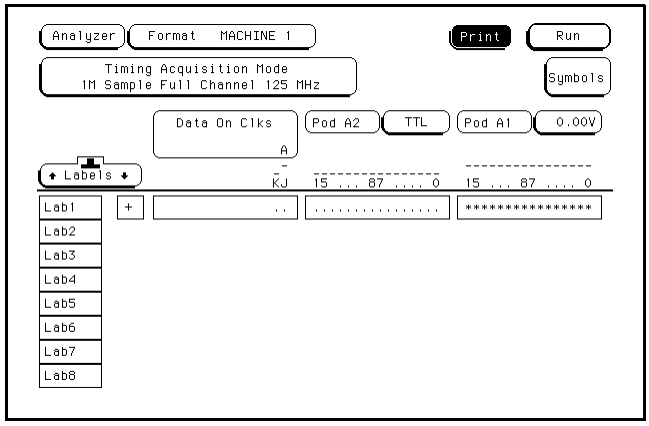
Test the 0 V User threshold

1. Move the cursor to the field to the right of Pod A1. Type 0, then press the Select key.
2. On the function generator front panel, enter +0.102 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4. Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



Test the next pod

1. Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator until all pods have been tested.

   To unassign a pod pair and assign the next pod pair to be tested, press the Config key. Select the pod pairs, then select assign or unassign in the pop-up menu.

2. Start with "Test the TTL threshold" on page 3–10, substituting the next pod to be tested for pod 1.

To test the single-clock, single-edge, state acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for single-clock, single-edge, state acquisition
- Minimum clock pulse width

This test checks two combinations of data channels using a single-edge clock at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948
Coupler	BNC(m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Doub: 10.0 ns	20.0 ns
Width: 3.5 ns	Width: 3.5 ns	
High: -0.9 V	High: -0.9 V	
Low: -1.7 V	Low: -1.7 V	

b Disable the pulse generator channel 2 COMP (with the LED off).

3 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

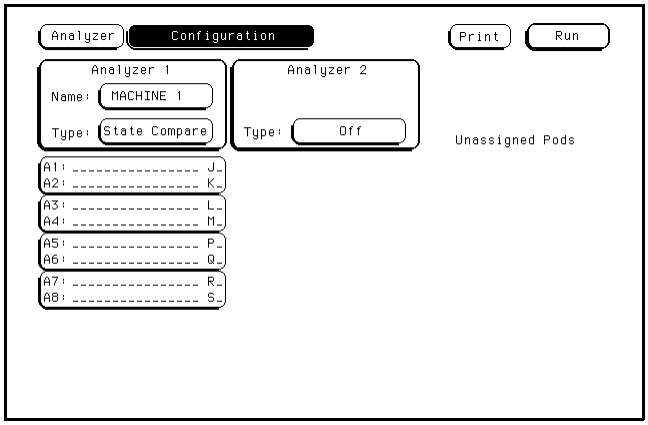
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign the pods, select the pod fields, then select Machine 1 in the pop-up menu.

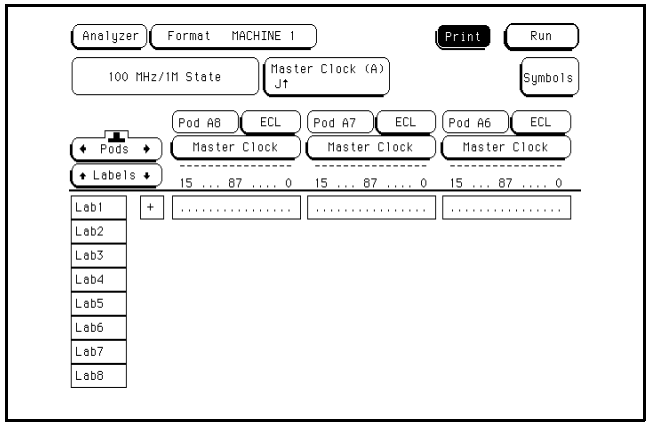
c Select the Type field in the Analyzer 1 box, then select State Compare.



2 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each pod, then select ECL in the pop-up menu. Use the knob to access pods not shown on the screen.



3 Set up the Trigger menu.

a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All in the pop-up menu.

b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

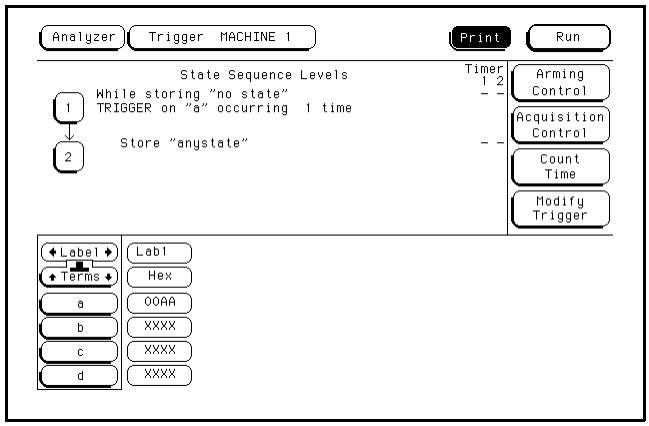
c Select Acquisition Control. If the Acquisition Control is "Manual," use the cursor keys to move the cursor to the Acquisition Model field. Press the "Select" key to toggle this field to "Automatic."

d In the Acquisition Control menu, use the knob to set the Memory Length to 4096. Press the Done key.

e Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate," then select "no state." Select Done to exit the State Sequence Levels menu.

f Select the field next to "a" under the label Lab1. Type the following for your logic analyzer, then press the Select key.

HP 1670D – "00AA" HP 1672D – "00AA" HP 1671D – "002A"



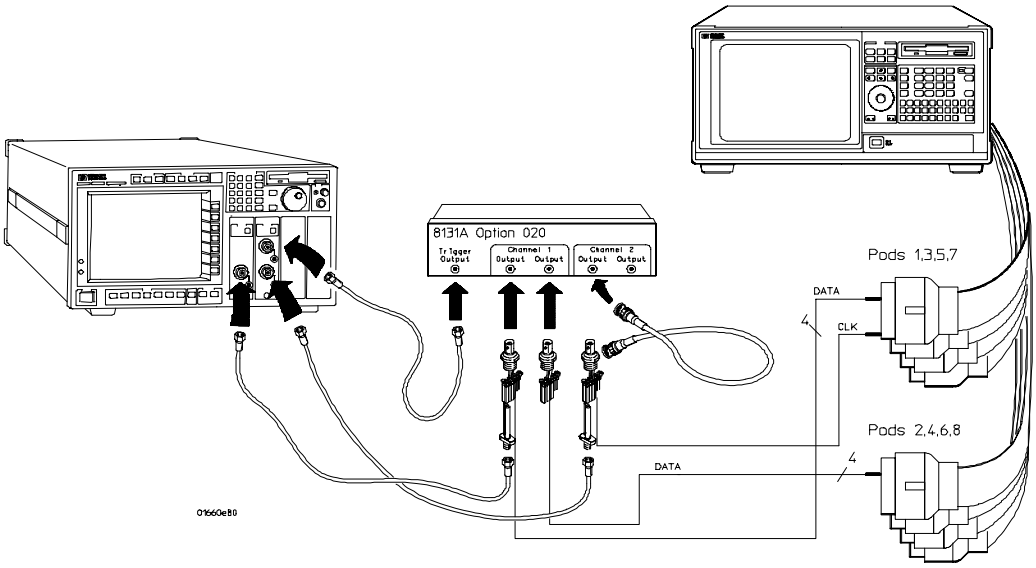
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an HP 1670D or HP 1671D, you will repeat this test for the second combination.

2 Using SMA cables, connect the oscilloscope to the pulse generator channel 1 Output, channel 2 Output, and Trig Output.

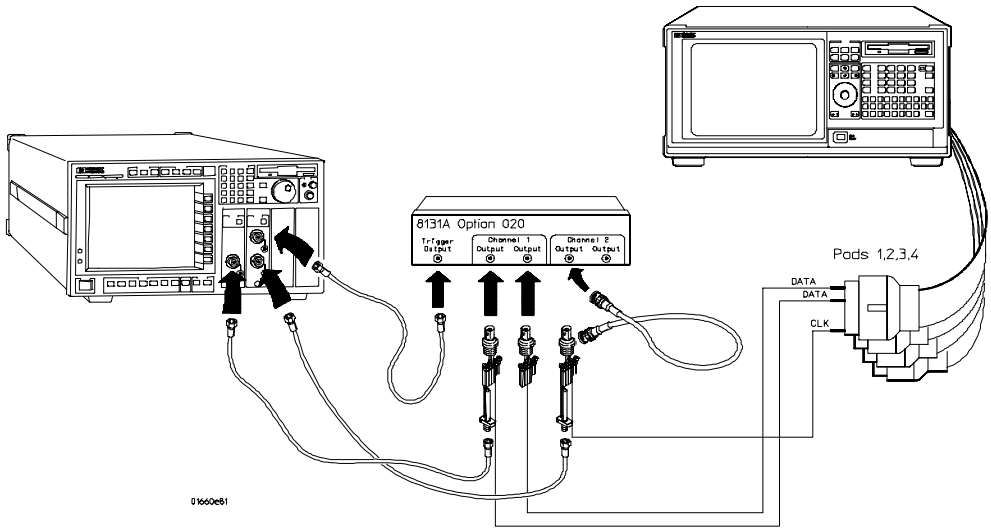
Connect the HP 1670D or HP 1671D Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 $\overline{\text{Output}}$	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3	J-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11	J-clock



Connect the HP 1672D Logic Analyzer to the Pulse Generator

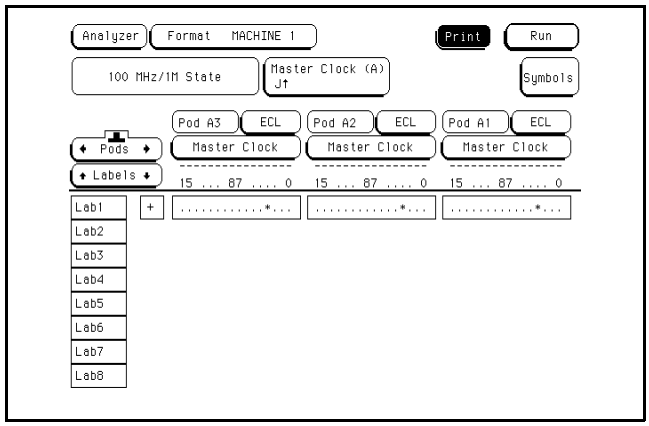
Testing Combination	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 $\overline{\text{Output}}$	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11 Pod 4, channel 11	J-clock



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested, then press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.



Verify the test signal

1 Check the clock pulse width. Using the oscilloscope, verify that the clock pulse width is 3.500 ns, +0 ps or −100 ps.

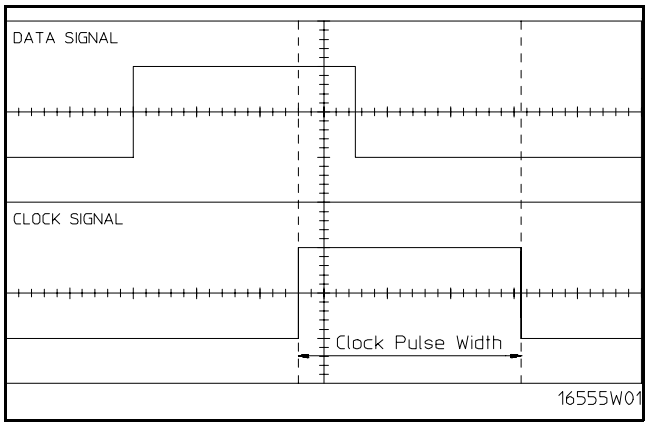
a Enable the pulse generator channel 1 and channel 2 outputs (LED off).

b In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.

d On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the clock signal pulse width (+ width(2)).

e If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



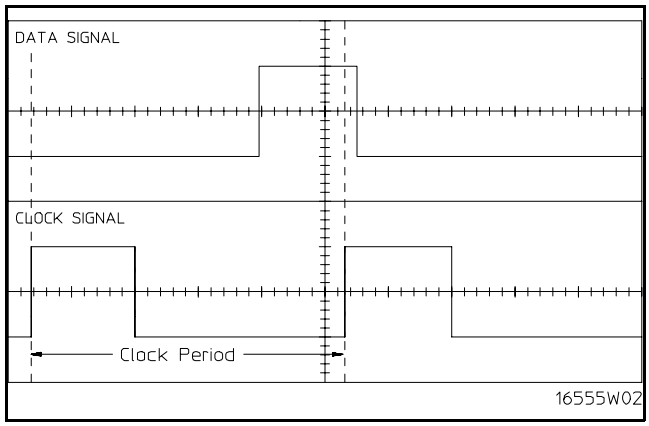
2 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or –200 ps.

a In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 10.000 ns, go to step d. If the period is less than 10.000 ns, go to step 3.

d In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is not less than 10.000 ns, decrease the pulse generator Chan 2 Doub in 10 ps increments until one of the two periods measured is less than 10.000 ns.



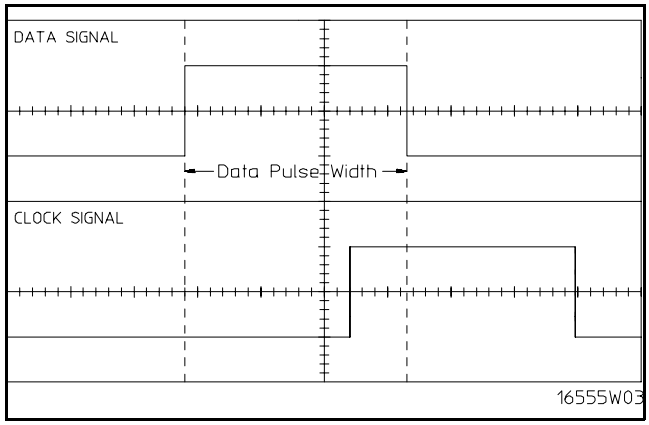
3 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.50 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the pulse width is within limits.



Check the setup/hold combination

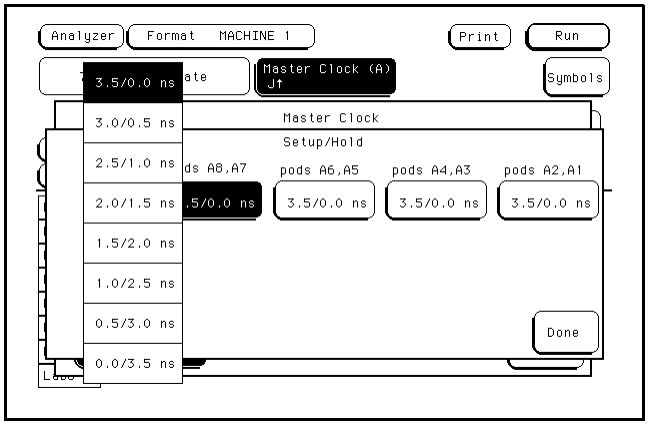
1 Select the logic analyzer setup/hold time.

a In the logic analyzer Format menu, select Master Clock.

b Select the Setup/Hold field, then select the setup/hold combination to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
3.5/0.0 ns
0.0/3.5 ns
1.5/2.0 ns

c Select Done to exit the setup/hold combinations.



2 Disable the pulse generator channel 2 COMP (with the LED off).

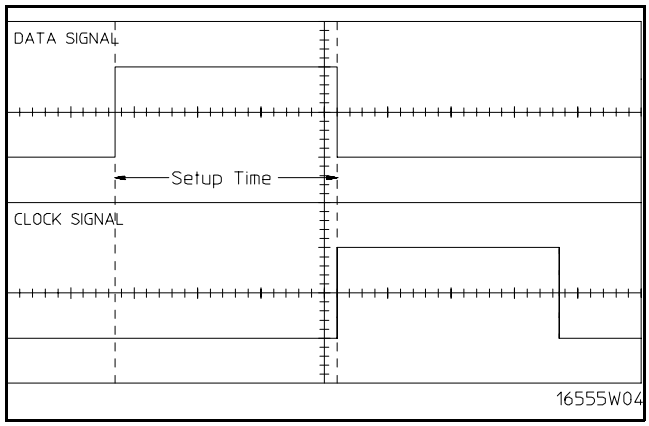
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



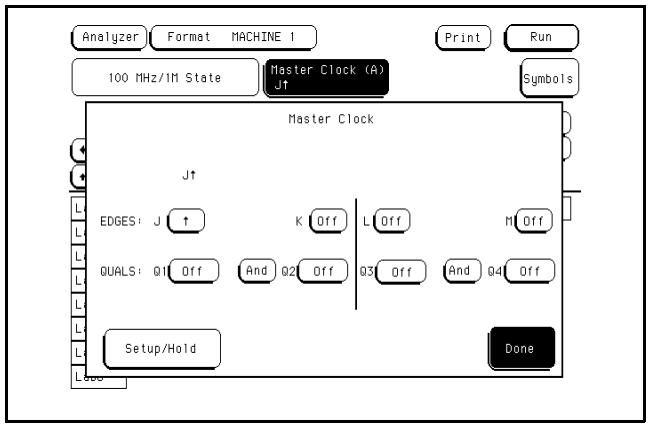
4 Select the clock to be tested.

a In the Master Clock menu, select the clock field to be tested, then select the clock edge as indicated in the table. The first time through this test, use the top clock and edge in the following table.

Clocks
J↑
K↑
L↑
M↑

b Connect the clock to be tested to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



5 Note: Do this step only the first time through the test, to create a Compare file. For subsequent runs, go to step 6. Use the following to create a Compare file:

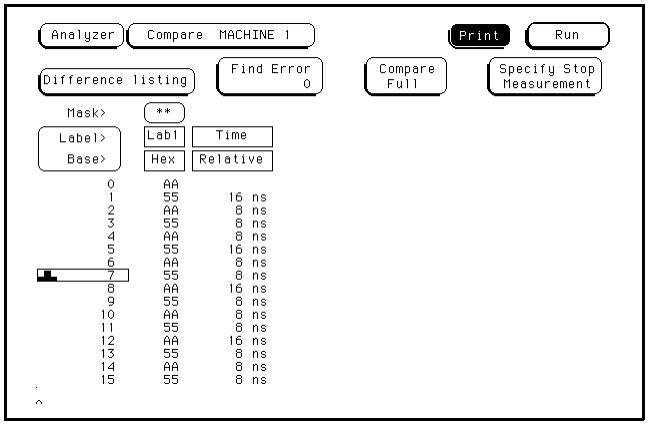
a Press Run. The display should show an alternating pattern of "AA" and "55." Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key. Select Execute.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop-up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop-up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



6 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

7 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 4, 6, and 7 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

8 Enable the pulse generator channel 2 COMP (with the LED on).

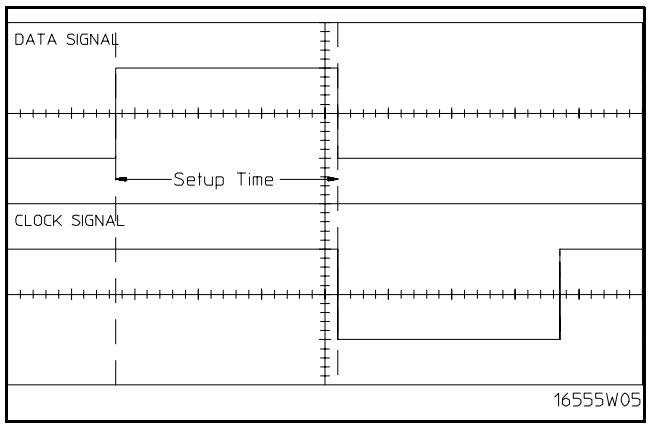
9 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] to verify the clock signal pulse width (- width(2)). If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the clock pulse width is 3.500 ns, +0 ps or -100 ps.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



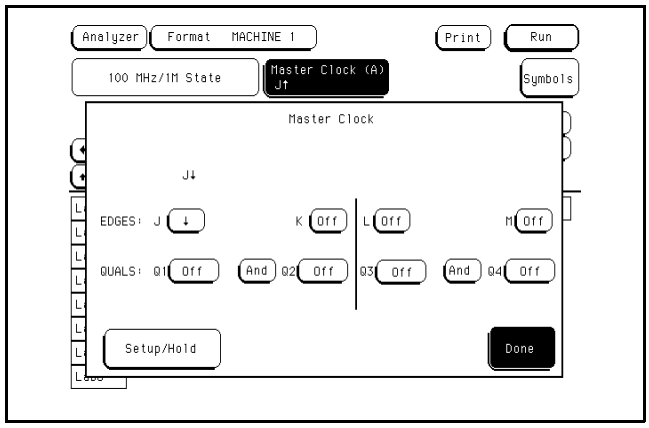
10 Select the clock to be tested.

a In the Master Clock menu, select the clock field to be tested, then select the clock edge as indicated in the table. The first time through this test, use the top clock and edge.

Clocks
J↓
K↓
L↓
M↓

b Connect the clock to be tested to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



11 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

12 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 10, 11, and 12 for the next clock edge listed in the table in step 11, until all listed clock edges have been tested.

13 Test the next setup/hold combination.

a In the logic analyzer Format menu, press Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 1 through 13 for the next setup/hold combination listed in step 1 on page 3–24, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

Connect the next combination of data channels and clock channels, then test them.

Start on page 3–20, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the multiple-clock, multiple-edge, state acquisition

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for multiple-clock, multiple-edge, state acquisition
- Minimum clock pulse width

This test checks two combinations of data using multiple clocks at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948
Coupler	BNC(m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Doub: 10.0 ns	20.0 ns
Width: 4.5 ns	Width: 3.5 ns	
High: –0.9 V	High: –0.9 V	
Low: –1.7 V	Low: –1.7 V	

b Disable the pulse generator channel 2 COMP (with the LED off).

3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

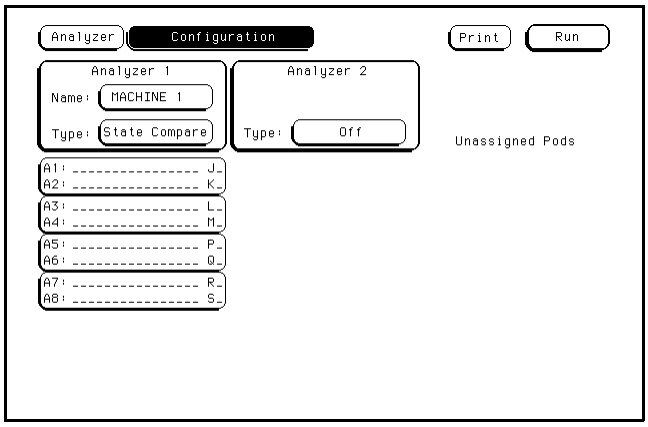
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign pods, select the pod fields, then select Machine 1.

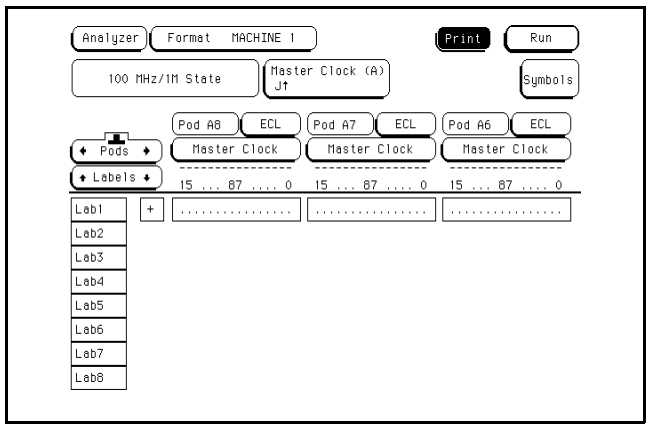
c In the Analyzer 1 box, select the Type field, then select State Compare.



2 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. Use the knob to access more Pod fields.



3 Set up the Trigger menu.

a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All in the pop-up menu.

b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

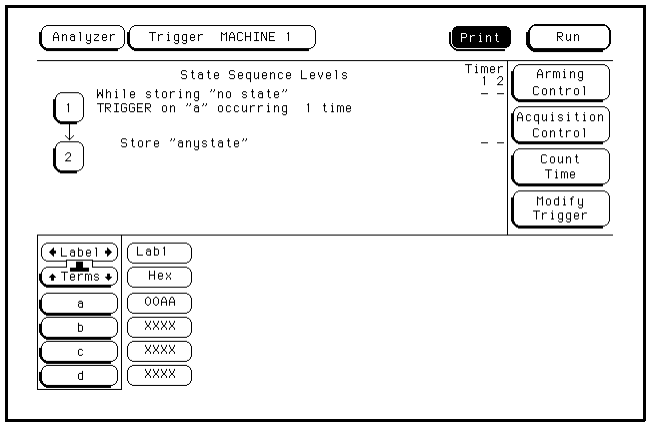
c Select Acquisition Control. If the Acquisition Control is "Manual," use the cursor keys to move the cursor to the Acquisition Model field. Press the "Select" key to toggle this field to "Automatic."

d In the Acquisition Control menu, use the knob to set the Memory Length to 4096. Press the Done key.

e Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate", then select "no state." Select Done to exit the State Sequence Levels menu.

f Select the field next to the pattern recognizer "a" under the label Lab1. Type the following for your logic analyzer, then press Select.

HP 1670D – "00AA" HP 1672D – "00AA" HP 1671D – "002A"



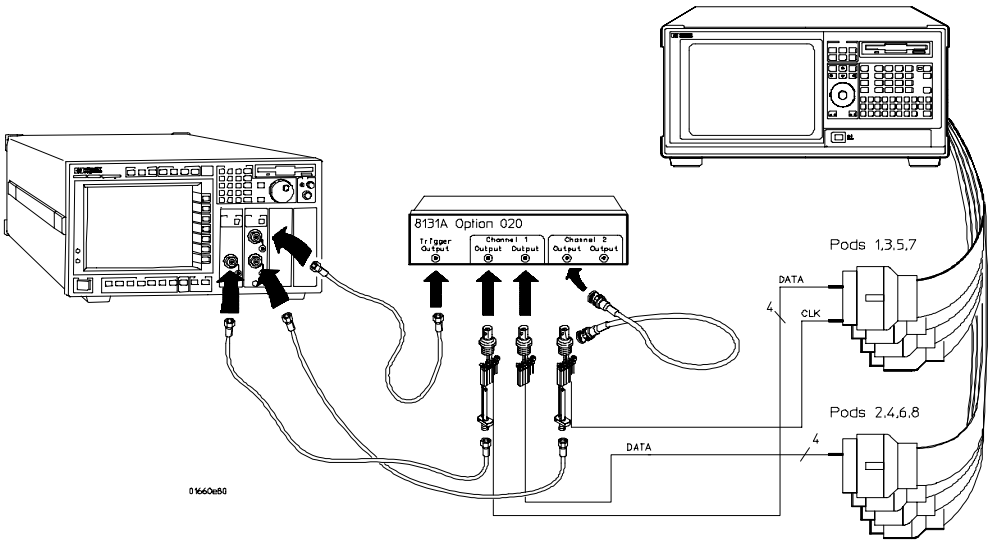
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an HP 1670D or HP 1671D, you will repeat this test for the second combination.

2 Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

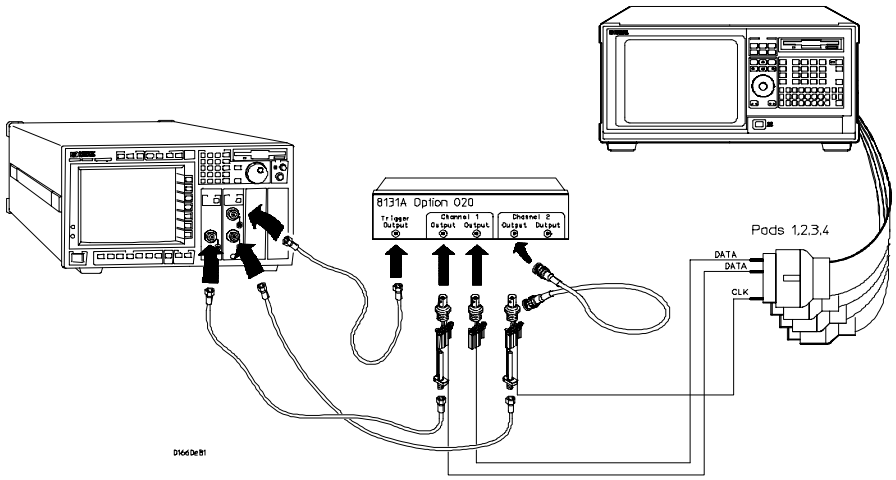
Connect the HP 1670D or HP 1671D Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 $\overline{\text{Output}}$	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3	J-clock K-clock L-clock M-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11	J-clock K-clock L-clock M-clock



Connect the HP 1672D Logic Analyzer to the Pulse Generator

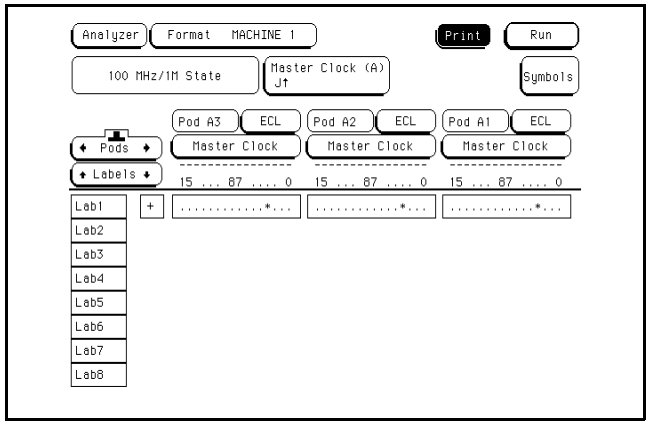
Testing Combination	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 $\overline{\text{Output}}$	Connect to HP 8131A Channel 2 Output	Connect to HP 8131A Channel 2 $\overline{\text{Output}}$
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11 Pod 4, channel 11	J-clock K-clock L-clock M-clock	



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

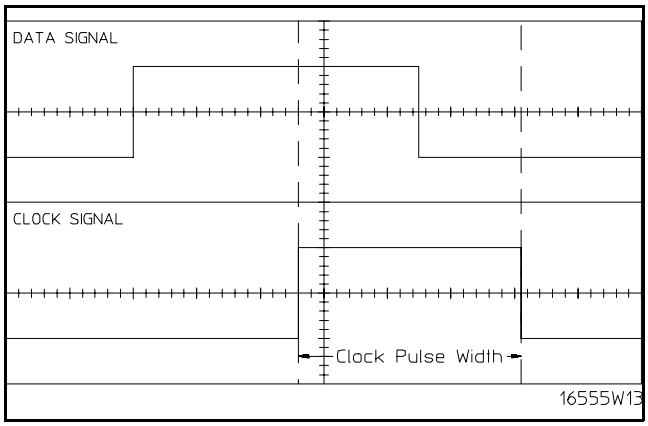
b Select the field showing the channel assignments for one of the pods being tested. Press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.



Verify the test signal

1 Check the clock pulse width. Using the oscilloscope, verify that the clock pulse width is 3.500 ns, +0 ps or −100 ps.

- **a** Enable the pulse generator channel 1 and channel 2 outputs (LED off).
- **b** In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.
- **d** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the clock signal pulse width (+ width (2)).
- **e** If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



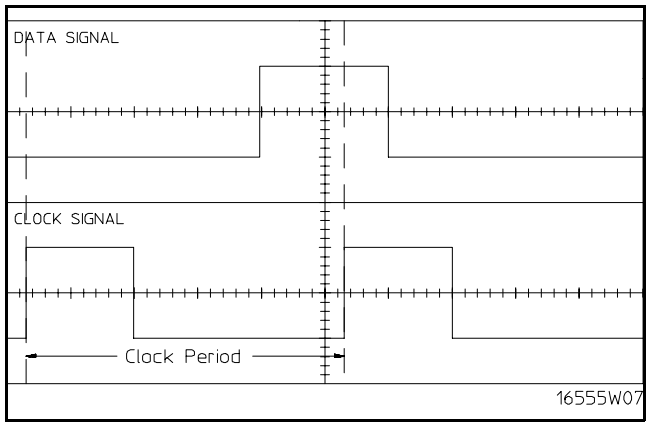
2 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or –200 ps.

a In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 10.000 ns, go to step d. If the period is less than 10.000 ns, go to step 3.

d In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is not less than 10.000 ns, decrease the pulse generator Chan 2 Doub in 10 ps increments until one of the two periods measured is less than 10.000 ns.



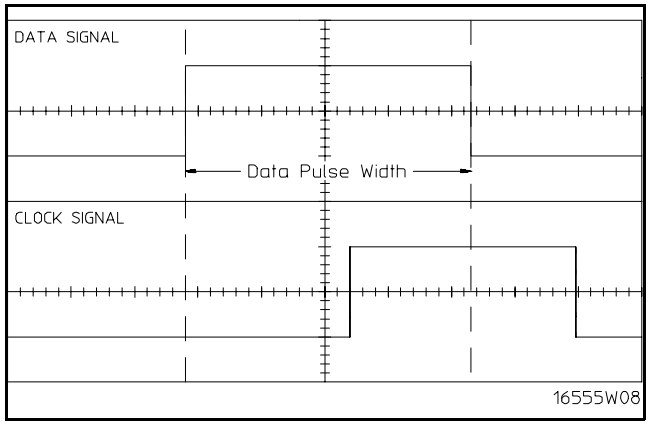
3 Check the data pulse width. Using the oscilloscope verify that the data pulse width is 4.500 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the pulse width is within limits.



Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

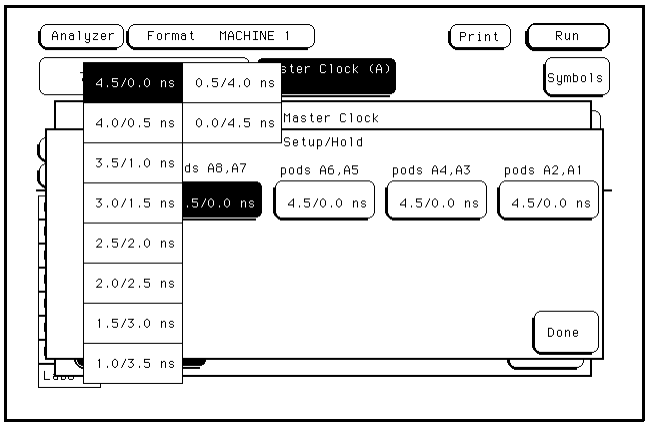
a In the logic analyzer Format menu, select Master Clock.

b Select and activate any two clock edges.

c Select the Setup/Hold field and select the setup/hold to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
4.5/0.0 ns
0.0/4.5 ns
2.0/2.5 ns

d Select Done to exit the setup/hold combinations.



2 Disable the pulse generator channel 2 COMP (with the LED off).

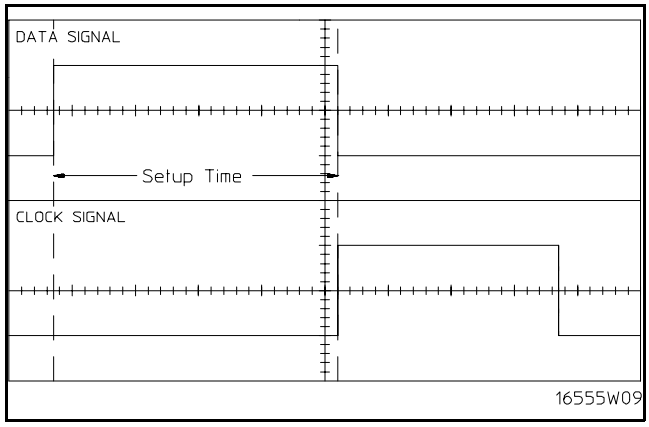
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



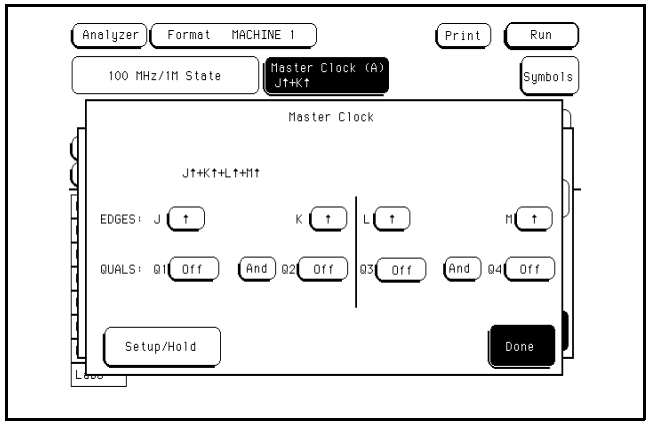
4 Select the clocks to be tested.

a Select the clock field to be tested and then select the clock edges as indicated in the table.

Clocks
J↑ + K↑ + L↑ + M↑

b Connect the rising edge clocks to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



5 If you have not already created a Compare file for the previous test (single-clock, single-edge state acquisition), use the following steps to create one. For subsequent passes through this test, skip this step and go to step 6.

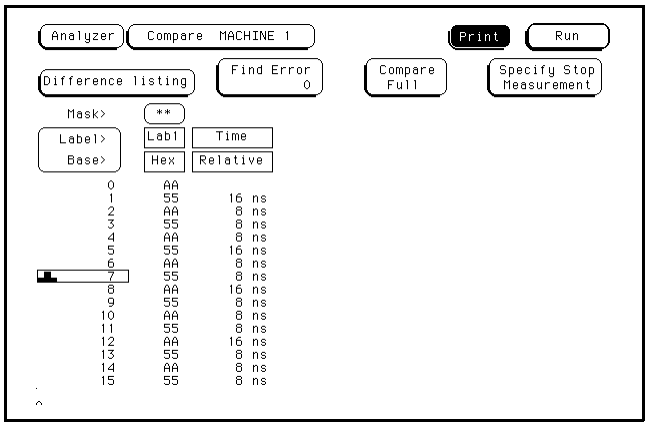
a Press Run. The display should show an alternating pattern of "AA" and "55." Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key. Select Execute.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop-up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop-up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



6 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

7 Enable the pulse generator channel 2 COMP (with the LED on).

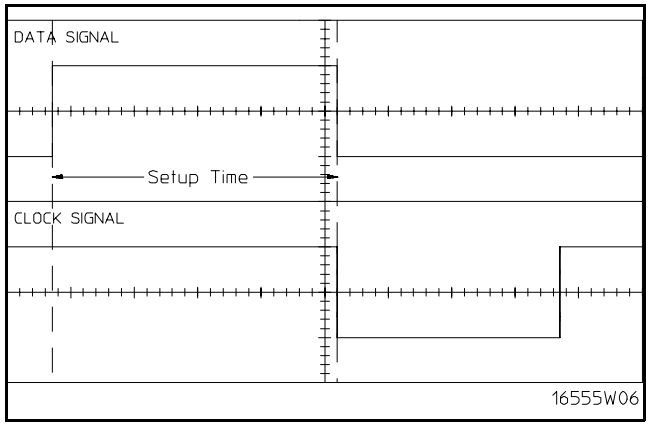
8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] to verify the clock signal pulse width (- width (2)). If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the clock pulse width is 3.500 ns, +0 ps or -100 ps.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

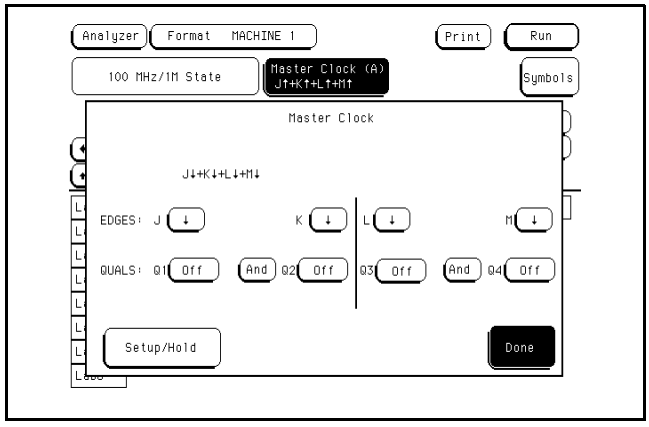


9 Select the clocks to be tested.

a Select the clock field to be tested, then select the clock edges as indicated in the table.

Clocks
J↓ + K↓ + L↓ + M↓

b Select Done to exit the Master Clock menu.



10 Press the blue shift key, then press the Run key. If two to four acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

11 Test the next clocks.

- **a** In the logic analyzer Format menu, select Master Clock.
- **b** Turn off and disconnect the clocks just tested.
- **c** Repeat steps 2 through 11 for the next clock edges listed in the table in step 4, until all listed clock edges have been tested.

12 Test the next setup/hold combination.

- **a** In the logic analyzer Format menu, select Master Clock.
- **b** Turn off and disconnect the clocks just tested.
- **c** Repeat steps 1 through 12 for the next setup/hold combination listed in step 1 on page 3-36, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

Connect the next combination of data channels and clock channels, then test them.

Start on page 3–32 "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the single-clock, multiple-edge, state acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for single-clock, multiple-edge, state acquisition
- Minimum clock pulse width

This test checks two combinations of data using a multiple-edge single clock at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948
Coupler	BNC(m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Delay: 0 ps	20.0 ns
Width: 4.0 ns	Dcyc: 50%	
High: –0.9 V	High: –0.9 V	
Low: –1.7 V	Low: –1.7 V	
COMP: Disabled (LED off)	COMP: Disabled (LED off)	

3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

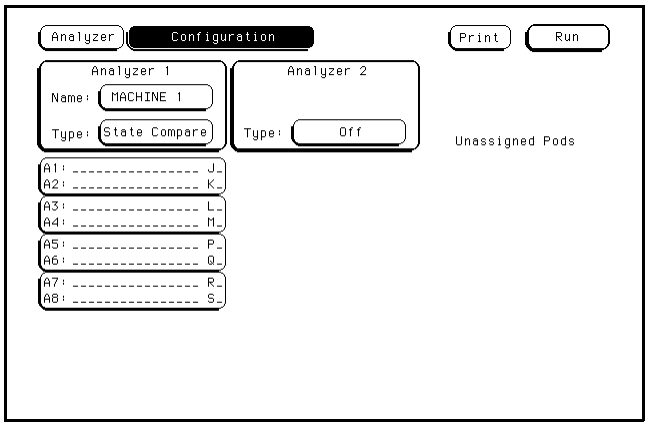
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign all pods, select the pod fields, then select Machine 1 in the pop-up menu.

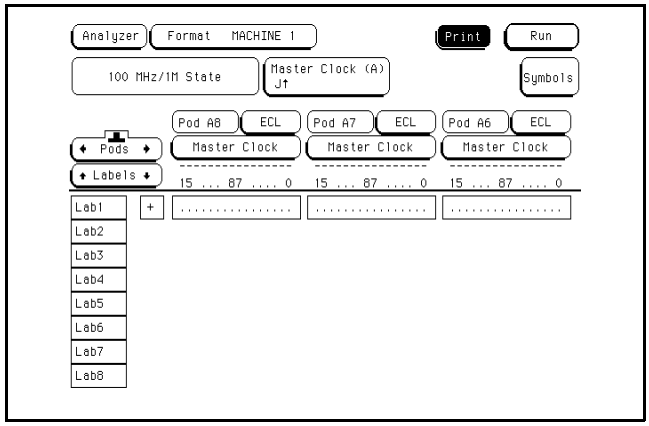
c Select the Type field in the Analyzer 1 box, then select State Compare.



2 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each pod field, then select ECL. The screen does not show all pod fields at one time. Use the knob to access pod fields not shown on the screen.



3 Set up the Trigger menu.

a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All in the pop-up menu.

b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

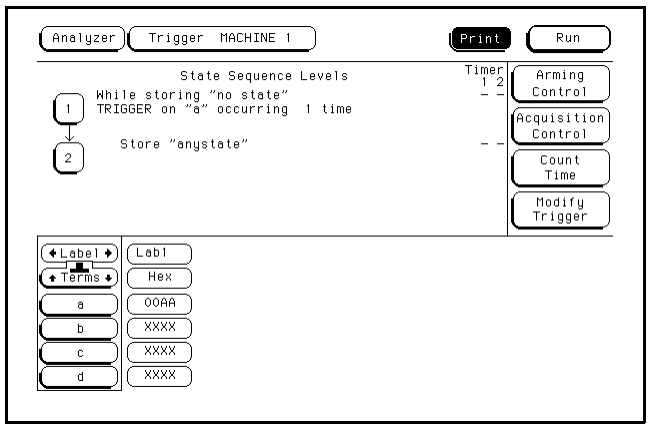
c Select Acquisition Control. If the Acquisition Control is "Manual," use the cursor keys to move the cursor to the Acquisition Model field. Press the "Select" key to toggle this field to "Automatic."

d In the Acquisition Mode menu, use the knob to set the Memory Length to 4096.

e Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate," then select "no state." Select Done to exit the State Sequence Levels menu.

f Select the field next to "a" under the label Lab1. Type the following for your logic analyzer, then press the Select key.

HP 1670D – "00AA" HP 1672D – "00AA" HP 1671D – "002A"



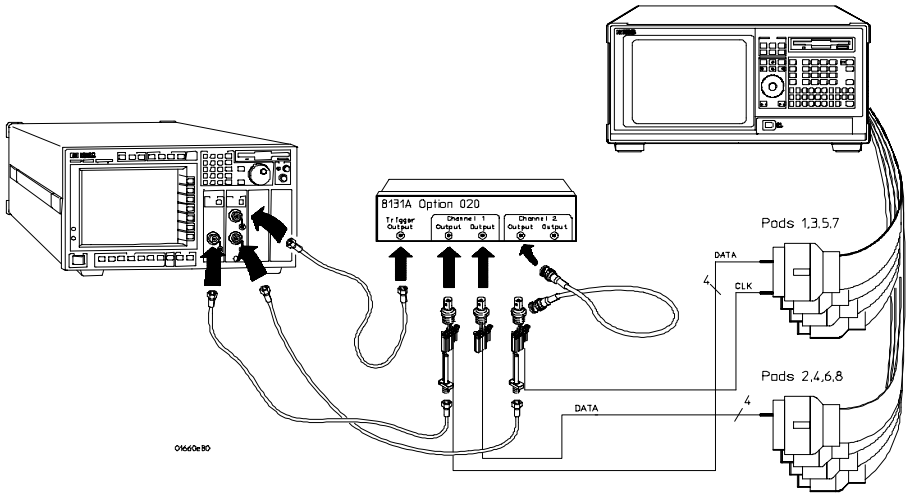
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an HP 1670D or HP 1671D, you will repeat this test for the second combination.

2 Using the SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

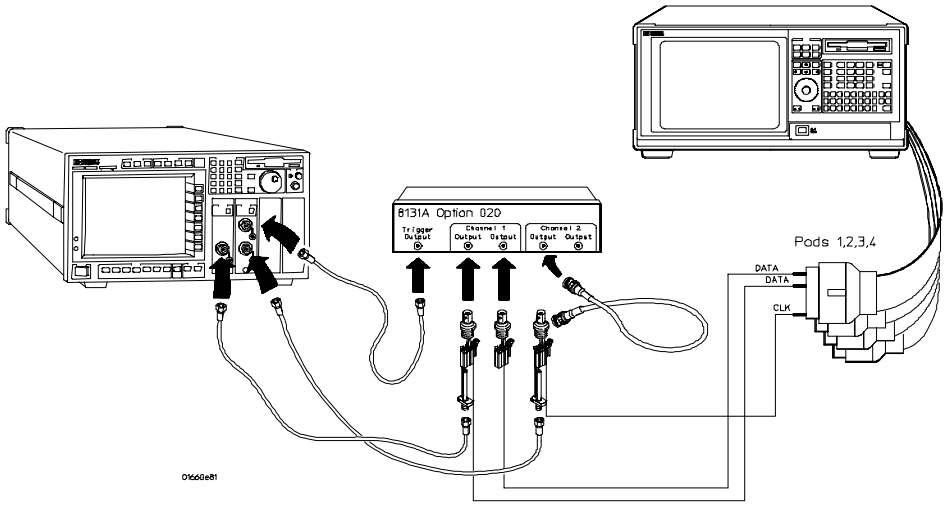
Connect the HP 1670D or HP 1671D Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 $\overline{\text{Output}}$	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3	J-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11	J-clock



Connect the HP 1672D Logic Analyzer to the Pulse Generator

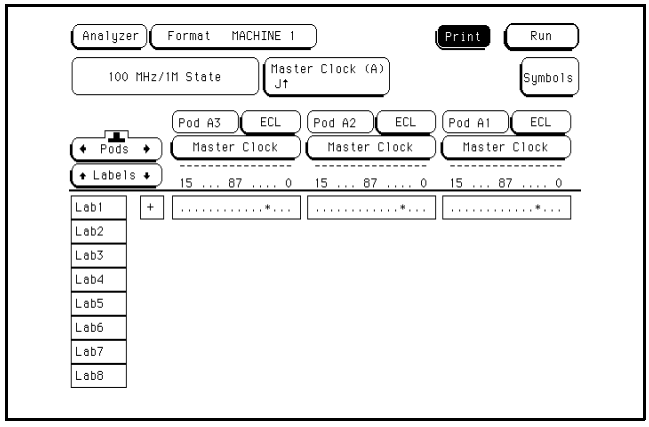
Testing Combination	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 $\overline{\text{Output}}$	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	J-clock



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested. Press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -200 ps.

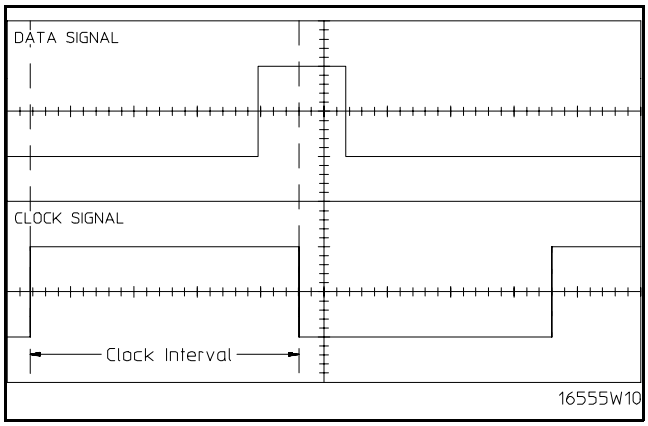
a In the oscilloscope Timebase menu, select Scale: 2.500 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 10.000 ns, go to step d. If the positive-going pulse width is less than or equal to 10.000 ns but greater than 9.900 ns, go to step 2.

d On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 10.000 ns but greater than 9.900 ns, go to step 2.

e Decrease the pulse generator Period in 100 ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 10.000 ns, but greater than 9.900 ns.



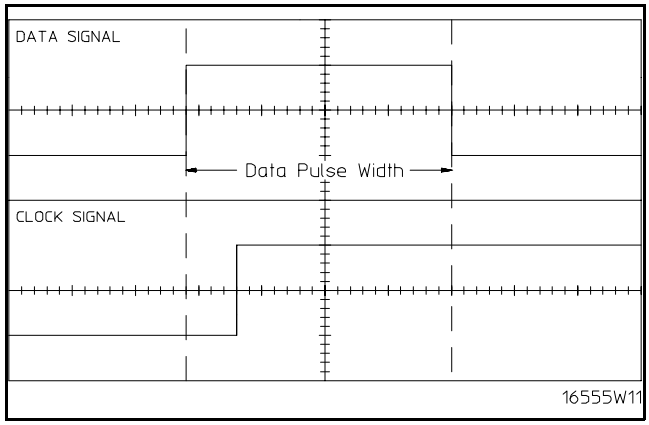
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the pulse width is within limits.



Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

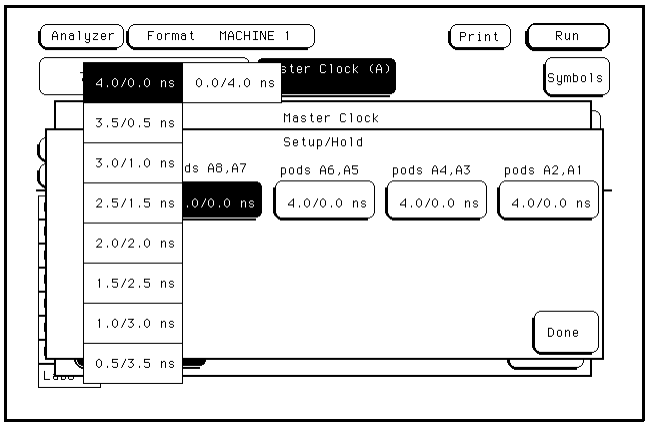
a In the logic analyzer Format menu, select Master Clock.

b Select and activate any multiple clock edge.

c Select the Setup/Hold field, then select the setup/hold to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
4.0/0.0 ns
0.0/4.0 ns
2.0/2.0 ns

d Select Done to exit the setup/hold combinations.



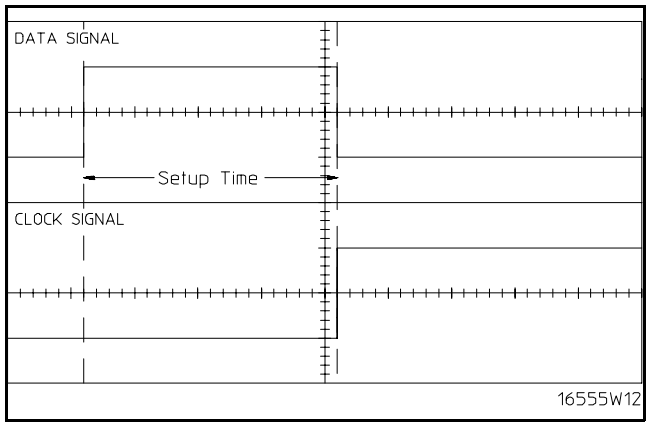
2 Using the Delay mode of the pulse generator channel 2, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 2 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



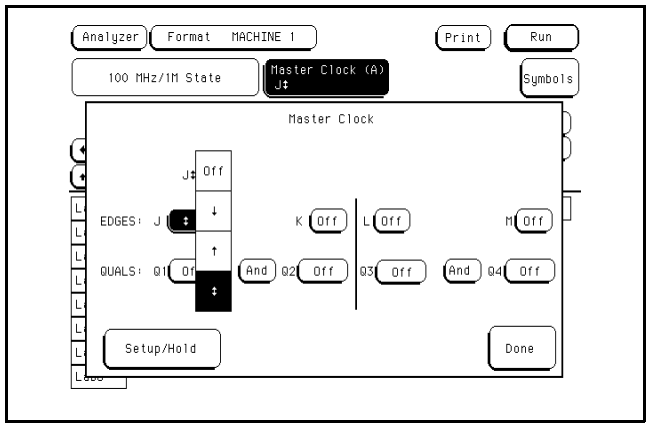
3 Select the clock to be tested.

a Select the clock field to be tested, then select the clock as indicated in the table. The first time through this test, use the top multiple-edge clock in the following table.

Clocks
J↕
K↕
L↕
M↕

b Connect the clock to be tested to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



4 If you have not already created a Compare file for one of the previous tests, use the following steps to create one. For subsequent passes through this test, skip this step and go to step 5.

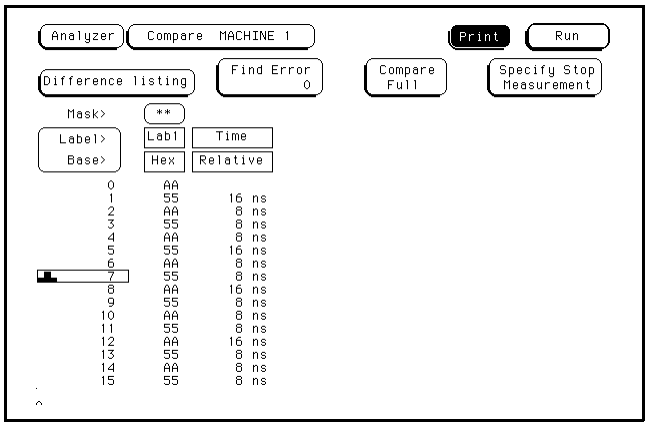
a Press Run. The display should show an alternating pattern of "AA" and "55." Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key. Select Execute.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop-up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop-up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



5 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

6 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 4, 6 and 7 for the next clock listed in the table in step 4, until all clocks have been tested.

7 Test the next setup/hold combination.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 1 through 10 for the next setup/hold combination listed in step 1 on page 3–48, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

- Connect the next combination of data channels and clock channels, then test them.

  Start on page 3–44, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the time interval accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125-MHz oscillator

This test verifies that the 125-MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100-MHz, 3.5-ns pulse width, < 600 ps rise time	HP 8131A Option 020
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency	HP 3325B Option 002
SMA Cable		HP 8120-4948
Adapter	BNC(m)-SMA(f)	HP 1250-2015
BNC Test Connector, 6x2		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Period	Mode	EXT TRIG
Delay: 0 ps	5 µs	TRIG	Slope: Positive
Width: 2.5 us			THRE: 1.0 V
High: –0.9 V			
Low: –1.7 V			
COMP: Disabled (LED off)			

3 Set up the function generator according to the following table.

Function Generator Setup	
Freq: 200 000.0 Hz	Main Function: Square wave
Amptd: 3.000 V	High Voltage: Disabled (LED Off)
Phase: 0.0 deg	
DC Offset: 0.0 V	

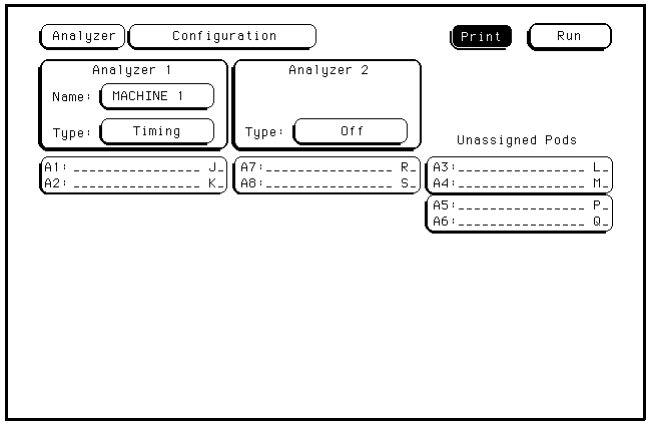
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign Pod 1 to Machine 1. To assign Pod 1, select the Pod 1 field, then select Machine 1.

c In the Analyzer 1 box, select the Type field, then select Timing.

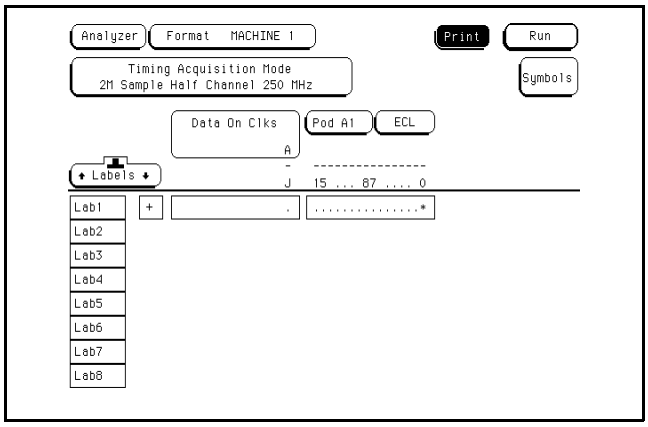


2 Set up the Format menu.

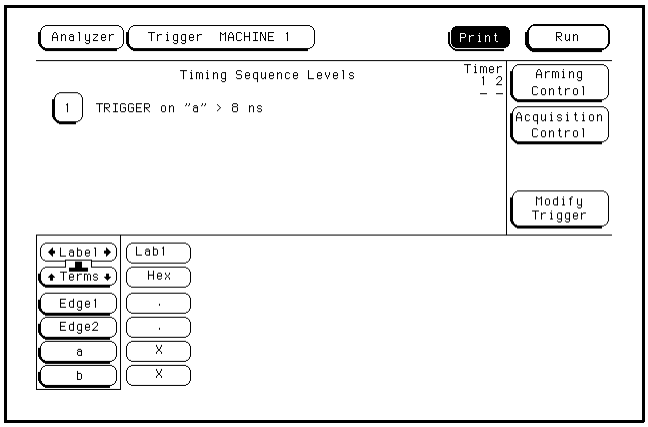
a Press the Format key. Select Timing Acquisition Mode, then select Half Channel 250 MHz.

b Select the field to the right of the Pod A1 field, then select ECL.

c Select the field showing the channel assignments for Pod A1. Deactivate all channels by pressing the Clear entry key. Using the arrow keys, move the selector to Channel 0. Press the Select key to put an asterisk in the channel position, activating the channel, then press the Done key.



3 Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All.



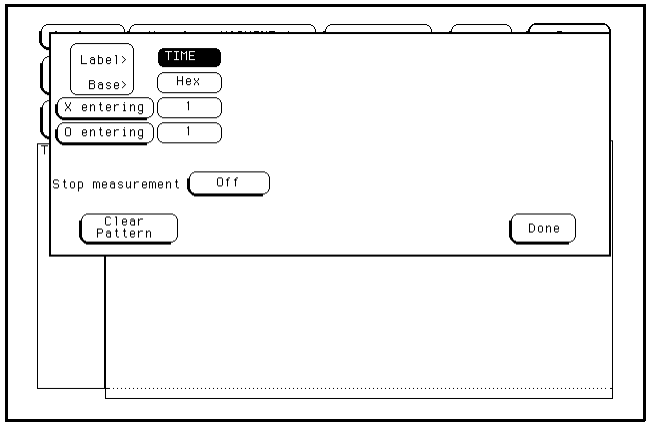
4 Set up the Waveform menu.

a Press the Waveform key.

b Move the cursor to the sec/Div field, then use the knob to dial in 2.00 µs.

c Select the Markers Off field, then select Pattern.

d Select the Specify Patterns field. Select X entering 1 and O entering 1.

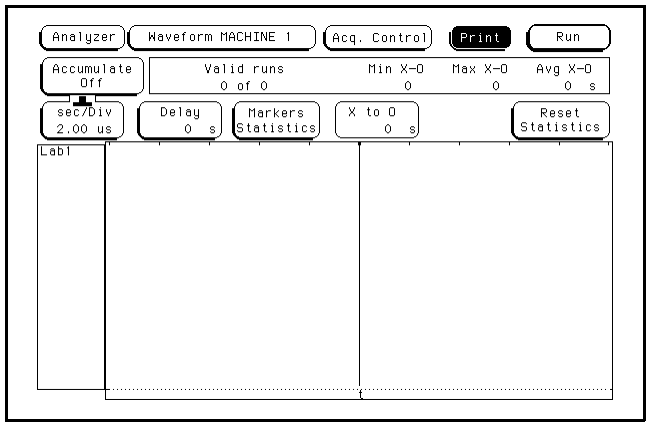


e Select Done to exit the Specify Patterns menu.

f Move the cursor to the X-pat field. Type 1, then press Done.

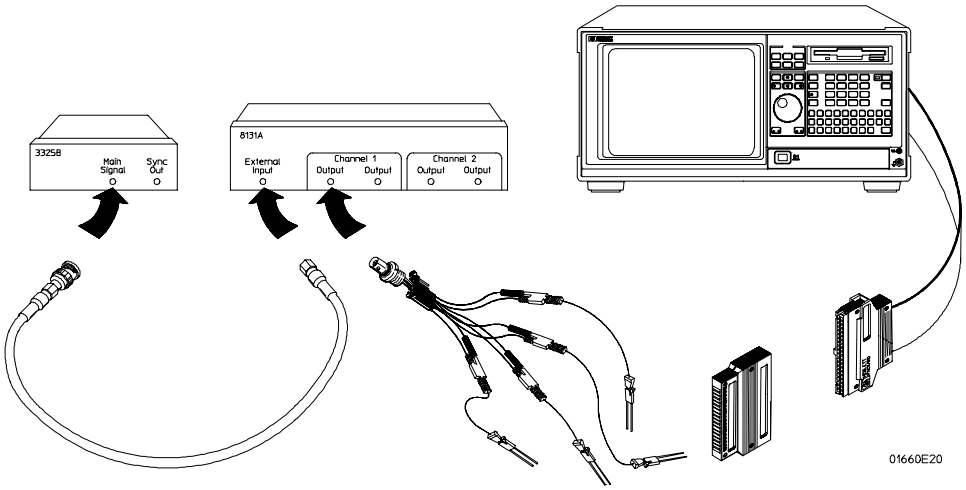
g Move the cursor to the O-pat field. Type 20, then press Done.

h Select the Markers Patterns field, then select Statistics. Select Reset Statistics to initialize the statistics fields.



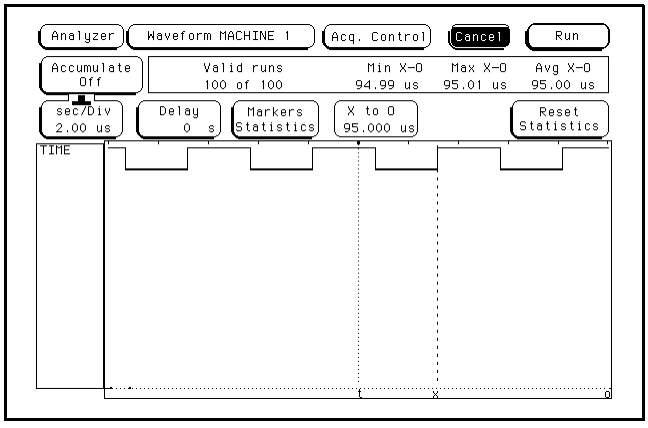
Connect the logic analyzer

1 Using a 6-by-2 test connector, connect channel 0 of Pod A1 to the pulse generator channel 1 output.
2 Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



Acquire the data

1 Enable the pulse generator channel 1 output (with the LED off).
2 Press the blue key, then press the Run key to select Run-Repetitive. Allow the logic analyzer to acquire data for at least 100 valid runs as indicated in the pattern statistics field.
3 When the logic analyzer has acquired at least 100 valid runs, select Stop. The Min X-O field in the logic analyzer Pattern Statistics menu should read 94.99–95.00 µs. The Max X-O field should read 95.00–95.01 µs. The Avg X-O field should read 94.99–95.01 µs. Record the results in the performance test record.



Performance Test Record

HEWLETT PACKARD

HP 1670D Series Logic Analyzer_____

Serial No._____ Work Order No._____

Recommended Test Interval - 2 Years/4000 hours Date_____

Recommended next testing_____ Temperature_____

Test	Settings		Results	
Self-Tests			Pass/Fail	_____
Threshold Accuracy	± (100 mV + 3% of threshold setting)			
			Limits	Measured
Pod 1	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 2	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 3	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

Performance Test Record (continued)

Test	Settings		Results	
Threshold Accuracy (cont'd)			Limits	Measured
Pod 4	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 5	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 6	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 7	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 8	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

Performance Test Record (continued)

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	3.5/0.0 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
	Setup/Hold Time	0.0/3.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
	Setup/Hold Time	1.5/2.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	3.5/0.0 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
	Setup/Hold Time	0.0/3.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
	Setup/Hold Time	1.5/2.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
Multiple-Clock, Multiple-Edge Acquisition			Enable pulse generator, channel 2 COMP (LED on)		Disable pulse generator, channel 2 COMP (LED off)	
				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.5/0.0 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
	Setup/Hold Time	0.0/4.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
	Setup/Hold Time	2.0/2.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
All Pods, Channel 11	Setup/Hold Time	4.5/0.0 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
	Setup/Hold Time	0.0/4.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
	Setup/Hold Time	2.0/2.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____

Performance Test Record (continued)

Test	Settings		Results	
Single-Clock, Multiple-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off)	
				Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.0/0.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
	Setup/Hold Time	0.0/4.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
	Setup/Hold Time	2.0/2.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	4.0/0.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
	Setup/Hold Time	0.0/4.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
	Setup/Hold Time	2.0/2.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
Time Interval Accuracy		Expected		Measured
	min X-0	94.99-95.00 µs		_____
	max X-0	95.00-95.01 µs		_____
	avg X-0	94.99-95.01 µs		_____

4

Calibrating and Adjusting

Calibrating and Adjusting

This chapter gives you instructions for calibrating and adjusting the logic analyzer. Adjustments to the logic analyzer include adjusting the CRT monitor assembly.

To periodically verify the performance of the analyzer, refer to "Testing Performance," chapter 3.

Logic analyzer calibration

The logic analyzer circuitry of the HP 1670D-series Logic Analyzers does not require an operational accuracy calibration. To test the logic analyzer circuitry against specifications (full calibration), refer to chapter 3, "Testing Performance."

To adjust the CRT monitor alignment

This procedure must be performed by trained personnel. Adjustments are made with the cover removed and power applied.

WARNING

Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.

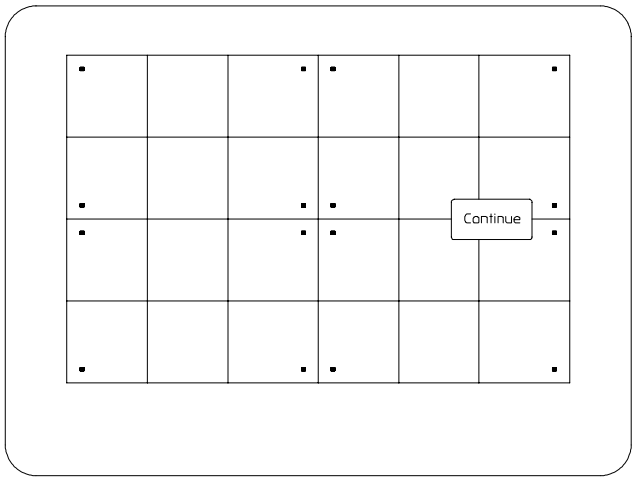
Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Alignment Tool	1	8710-1300

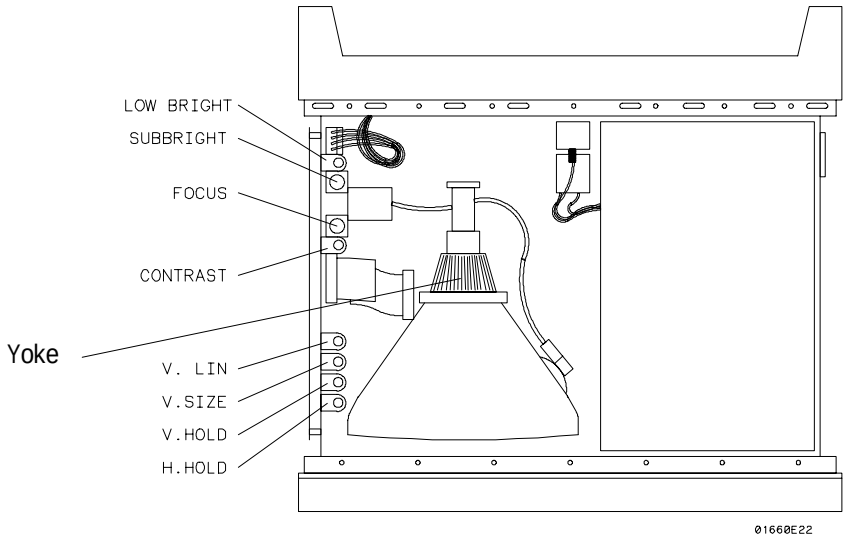
1. Turn off the logic analyzer, then disconnect the power cord. Remove the cover. Refer to chapter 6, "Replacing Assemblies," for instructions to remove the cover.
2. Connect the power cord, then turn on the logic analyzer.
3. Insert the disk containing the functional performance verification tests into the disk drive, then load the functional performance verification operating system into the logic analyzer.

4 Enter the Sys PV tests, then enter the Display Test.

A grid pattern should appear.



5 If the display is tilted (rotated), adjust the CRT yoke by rotating it to straighten the display.



6 If the grid pattern is not centered horizontally, adjust the H-Hold.

7 If you need to adjust the intensity, go to the next page.

If you are finished with the adjustments, turn off the instrument, then remove the power cord. Install the cover on the instrument.

To adjust the CRT intensity

This procedure must be performed by trained personnel. Adjustments are made with the cover removed and power applied.

WARNING

Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.

Equipment Required

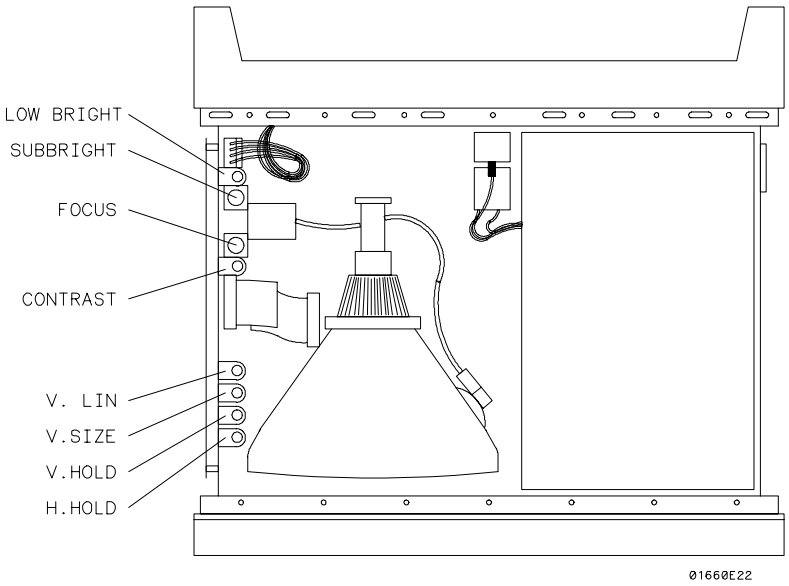
Equipment	Critical Specification	Recommended Model/Part
Alignment Tool	1	8710-1300
Light Power Meter		United Detector 351

If you just finished adjusting the CRT monitor alignment, go to step 4.

1. Turn off the logic analyzer, then disconnect the power cord. Remove the cover. Refer to chapter 6, "Replacing Assemblies," for instructions to remove the cover.
2. Connect the power cord, then turn on the logic analyzer.
3. Access the Display Test.
   a. Insert the disk containing the functional performance verification tests into the disk drive, then load the functional performance verification operating system into the logic analyzer.
   b. Enter the Sys PV tests and enter the Display Test. A grid pattern should appear.
4. Press the front-panel Select key.
   The display should show a full bright test screen.
5. Turn the rear panel intensity adjustment to full bright.
6. Place the light power meter against the display at center screen.

WARNING Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.

7 The light power meter should read 137-154 cd/m^2. If the measurement is out of this range, use the adjustment tool to adjust the Contrast potentiometer on the monitor driver board.



8 Press the front panel Select key.

The display should show a half bright test screen.

9 Place the light power meter against the display at center screen. The light power meter should read 5-27 cd/m^2.

If the reading is not correct, try adjusting the contrast in step 7 closer to the limit.

10 Press the front panel Select key.

The logic analyzer should exit the Display Test.

11 Place the light power meter against the display at center screen. Adjust the rear panel intensity adjustment until the light power meter reads 45-55 cd/m^2.

12 Exit the functional performance verification tests.

13 Turn off the instrument, then remove the power cord. Install the cover on the instrument.

5

Troubleshooting

Troubleshooting

This chapter helps you troubleshoot the logic analyzer to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, and tests. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests.

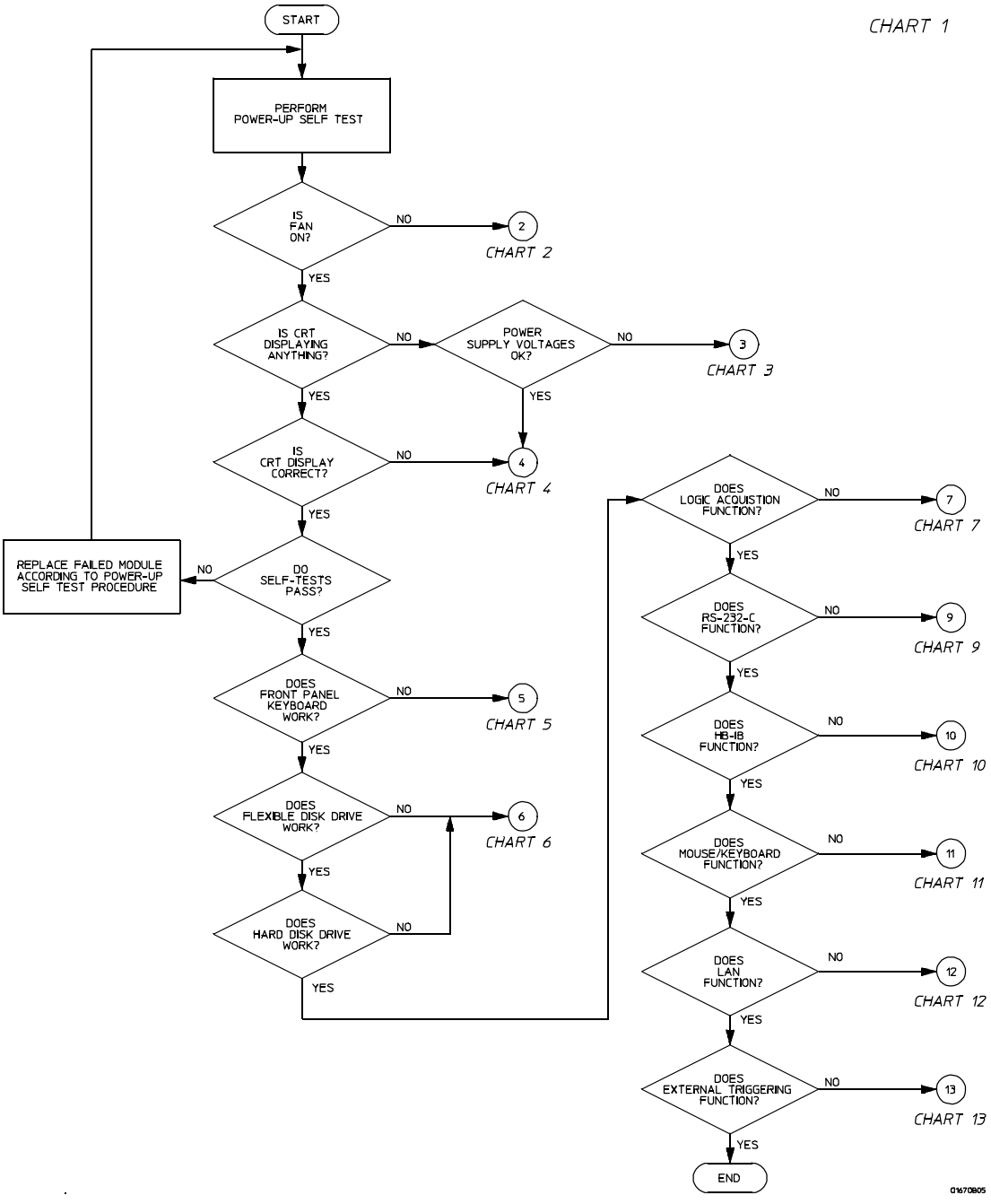
The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.

CAUTION

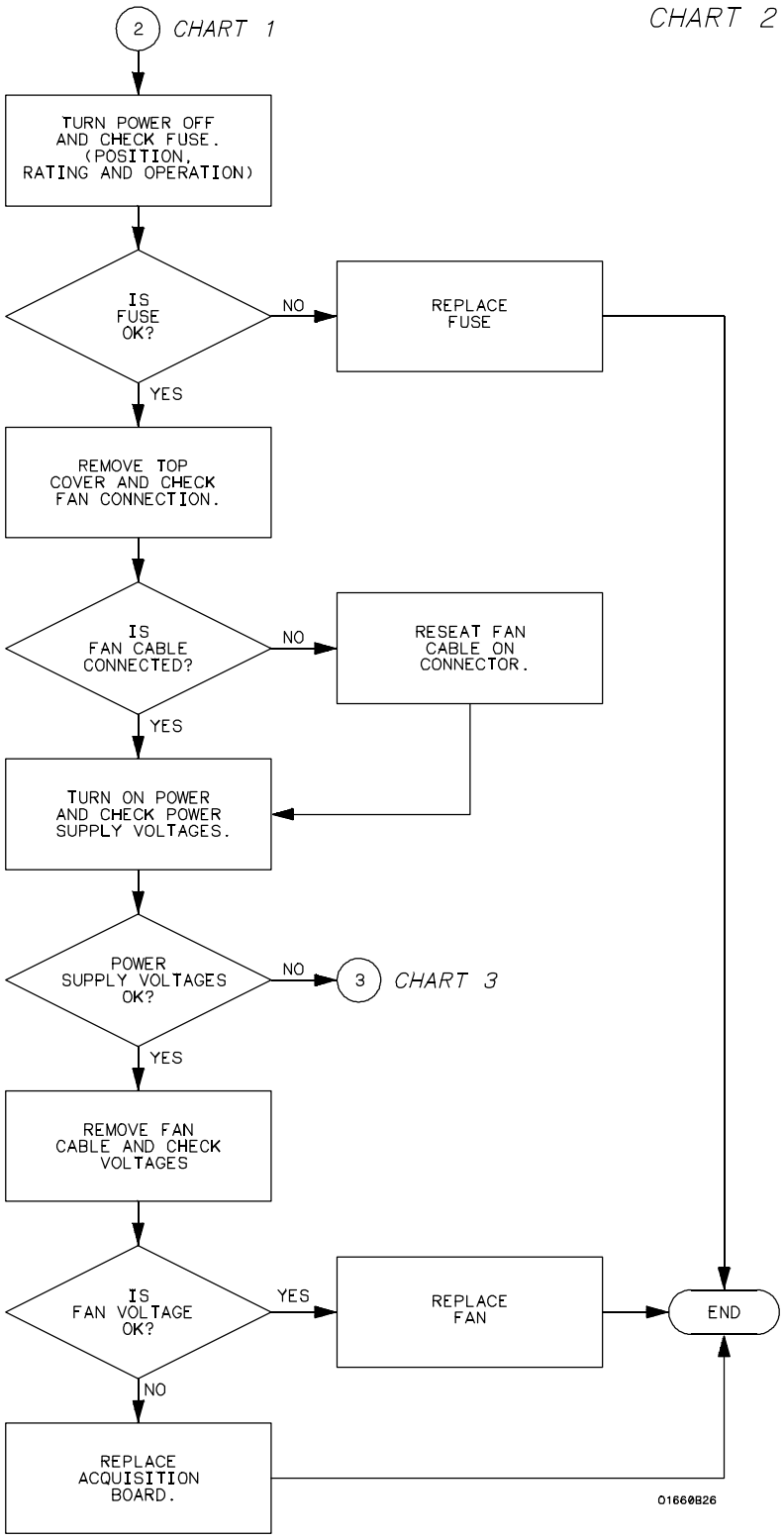
Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

To use the flowcharts

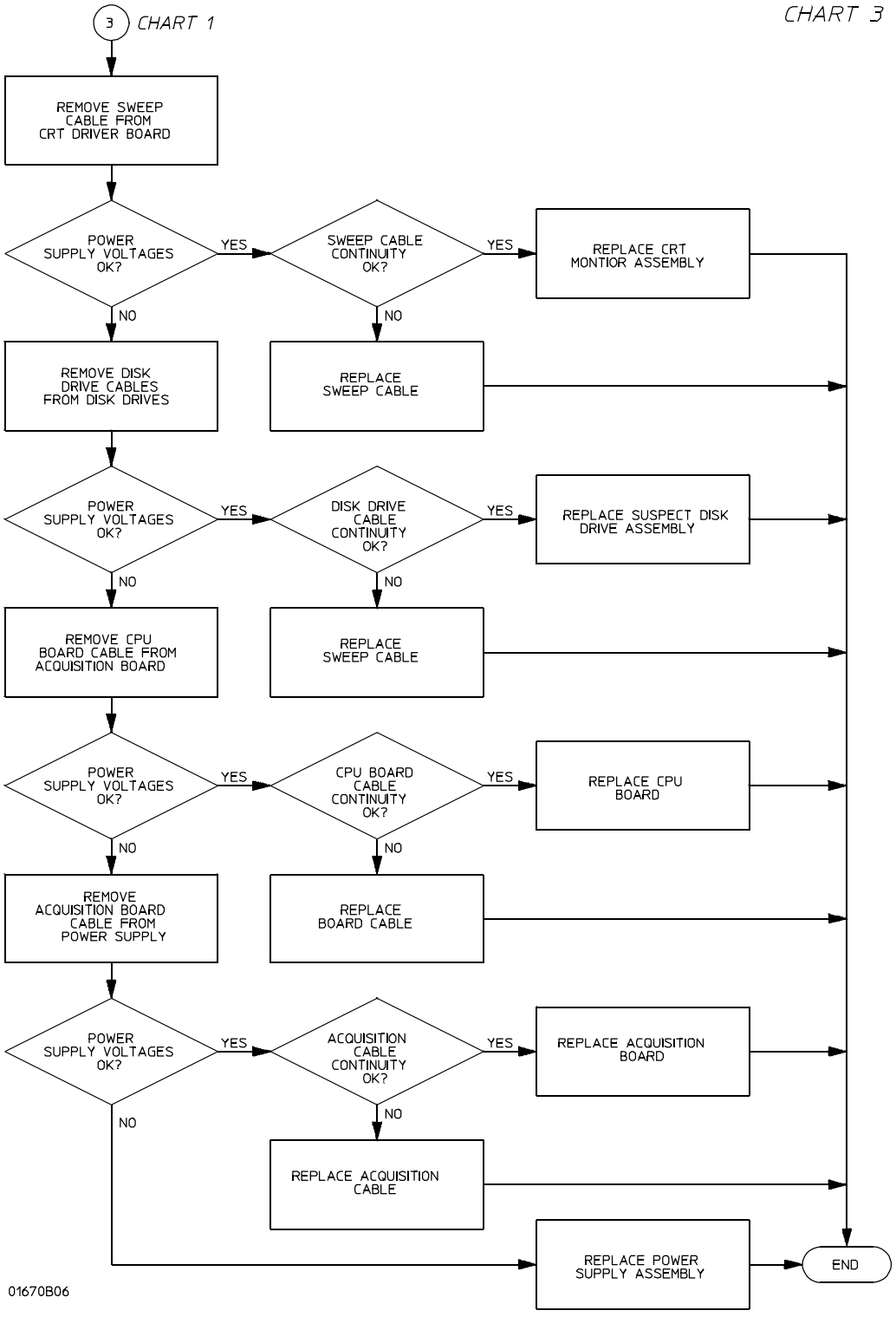
Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.



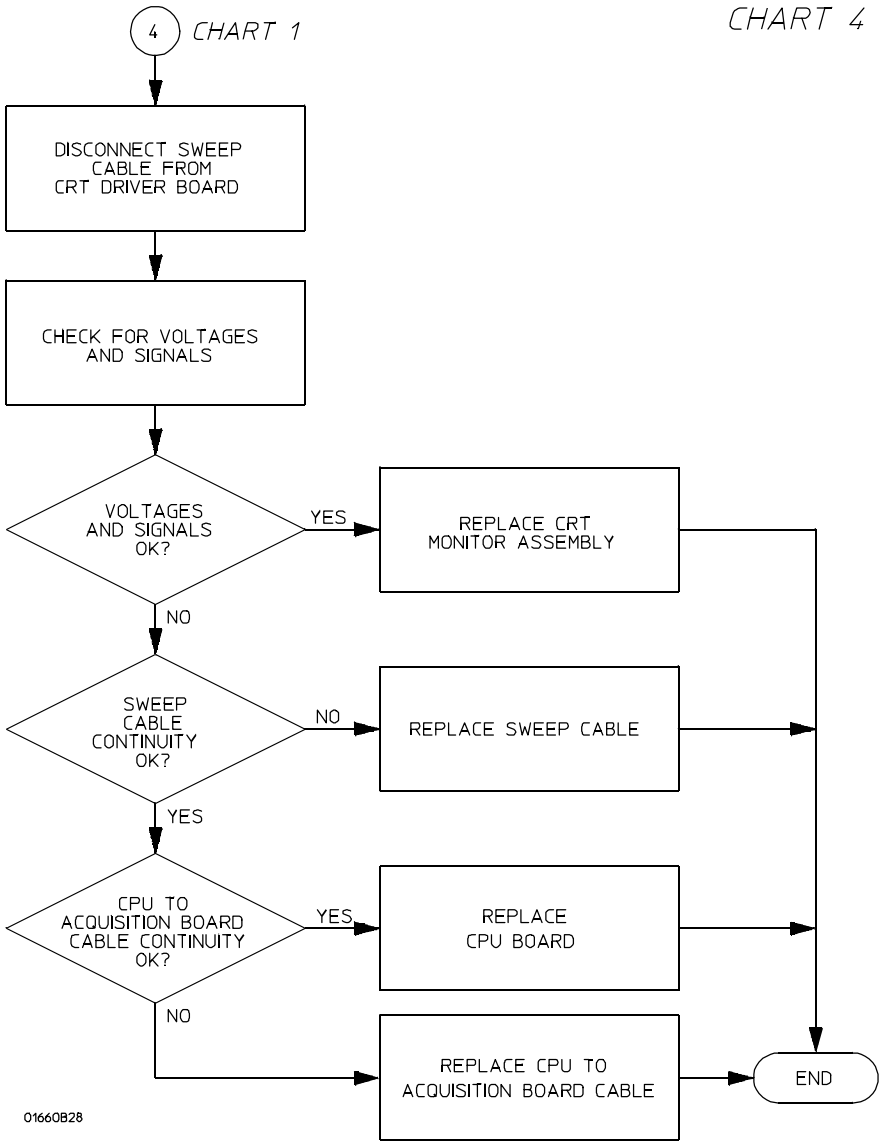
Troubleshooting Flowchart 1



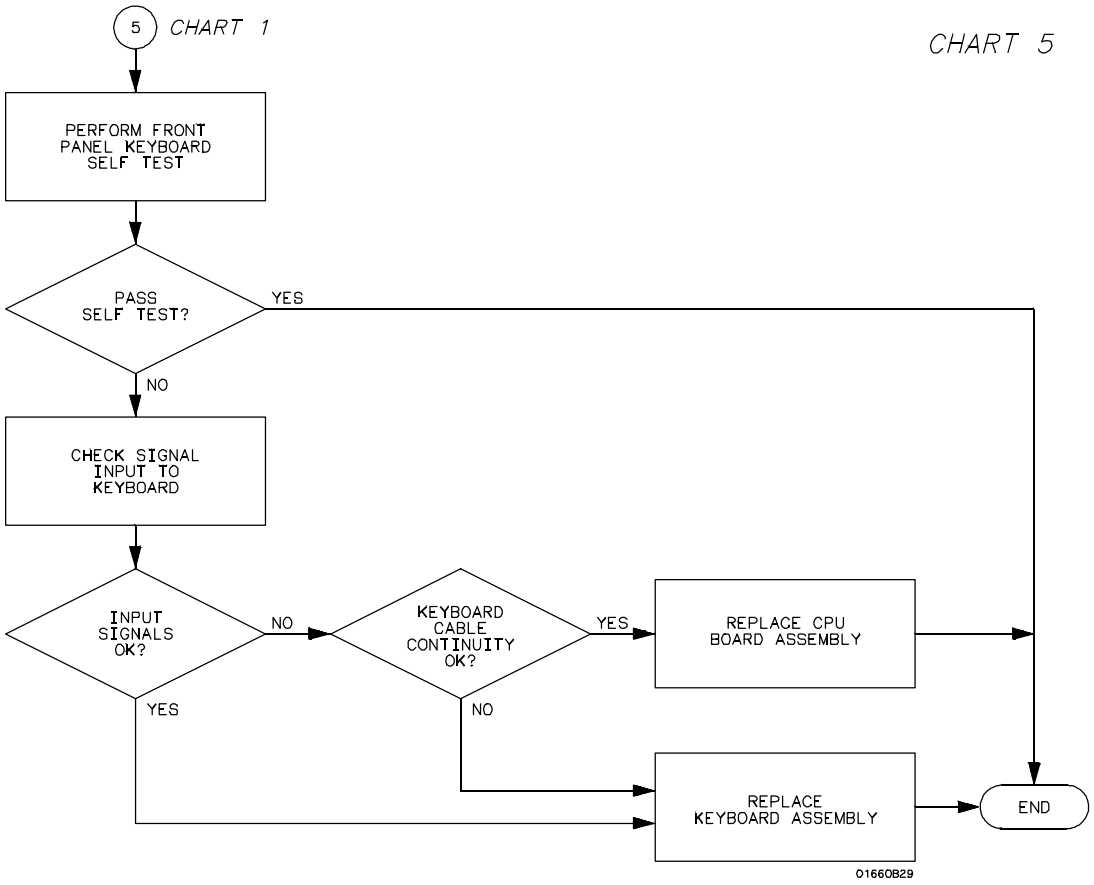
Troubleshooting Flowchart 2



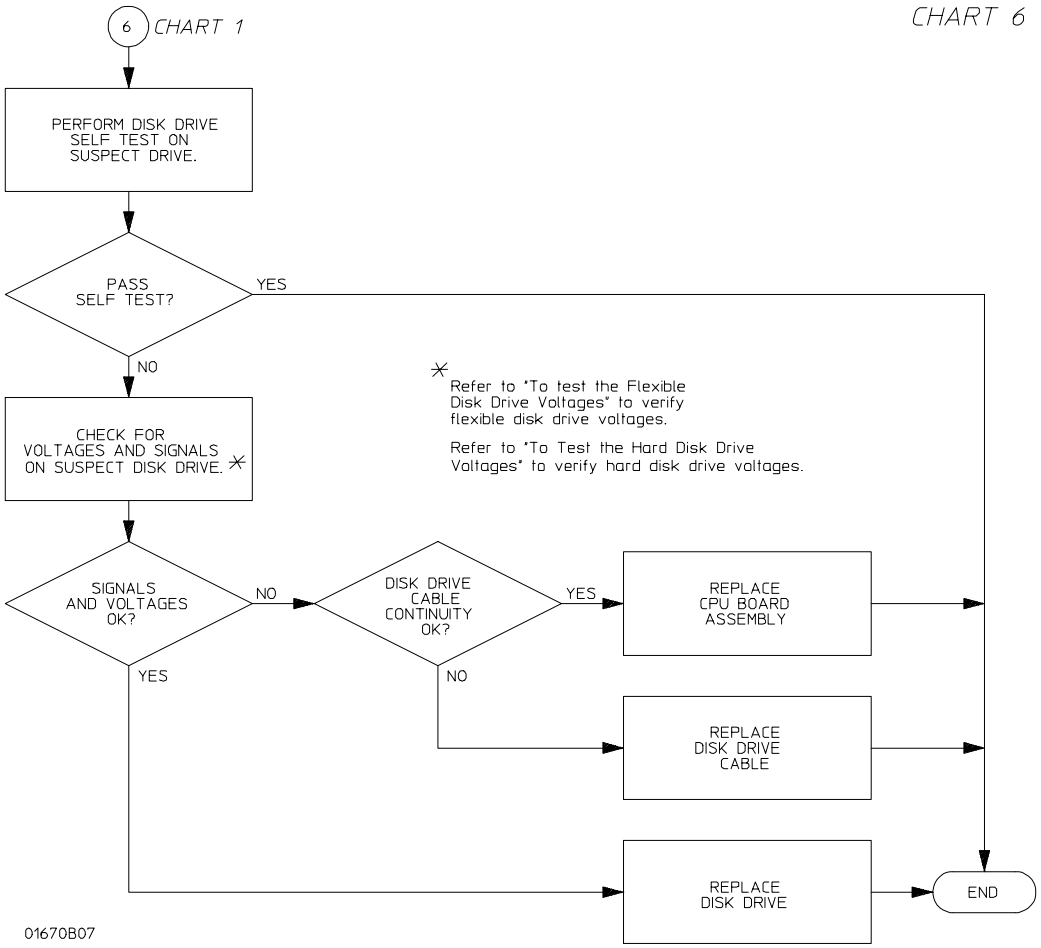
Troubleshooting Flowchart 3



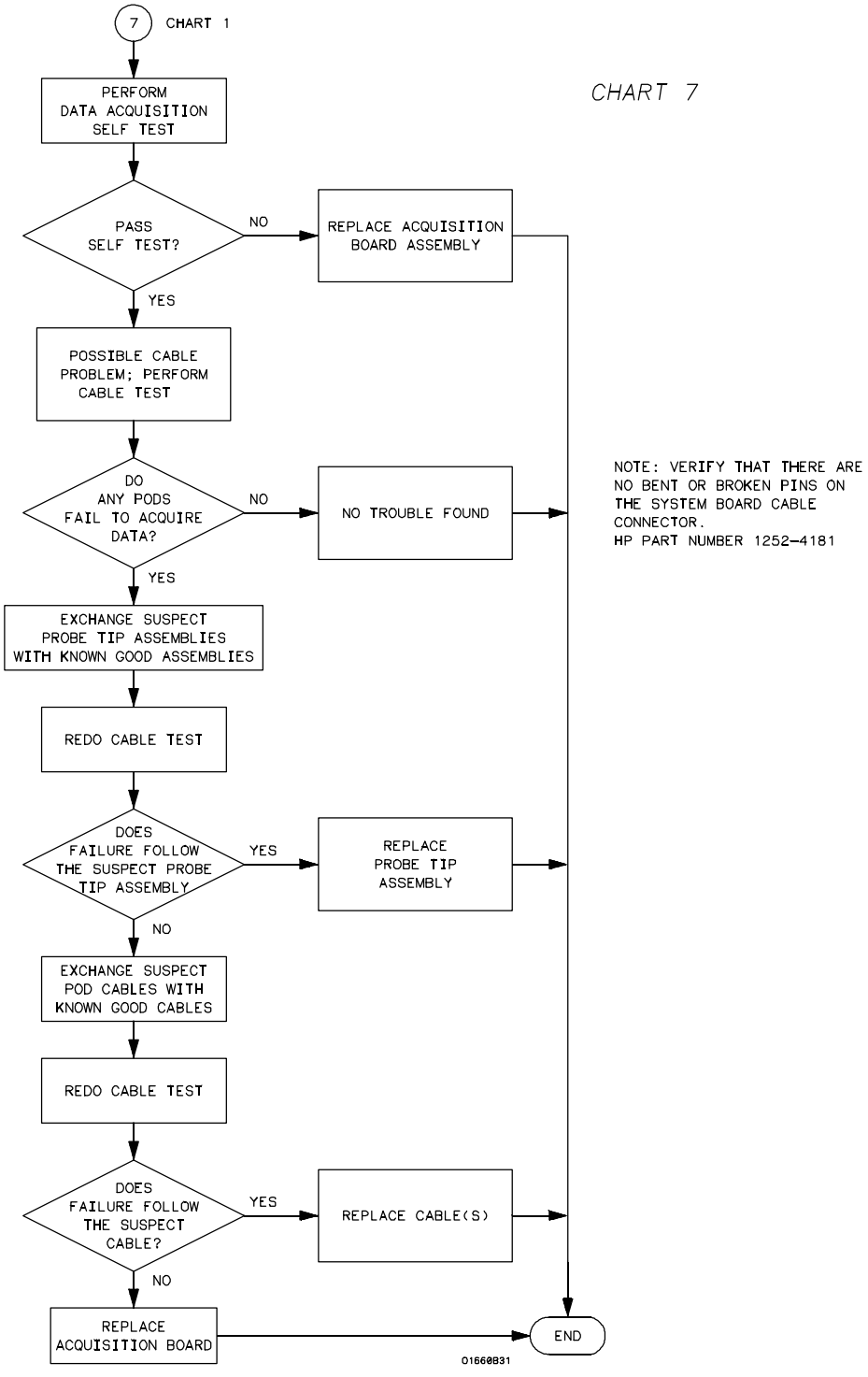
Troubleshooting Flowchart 4



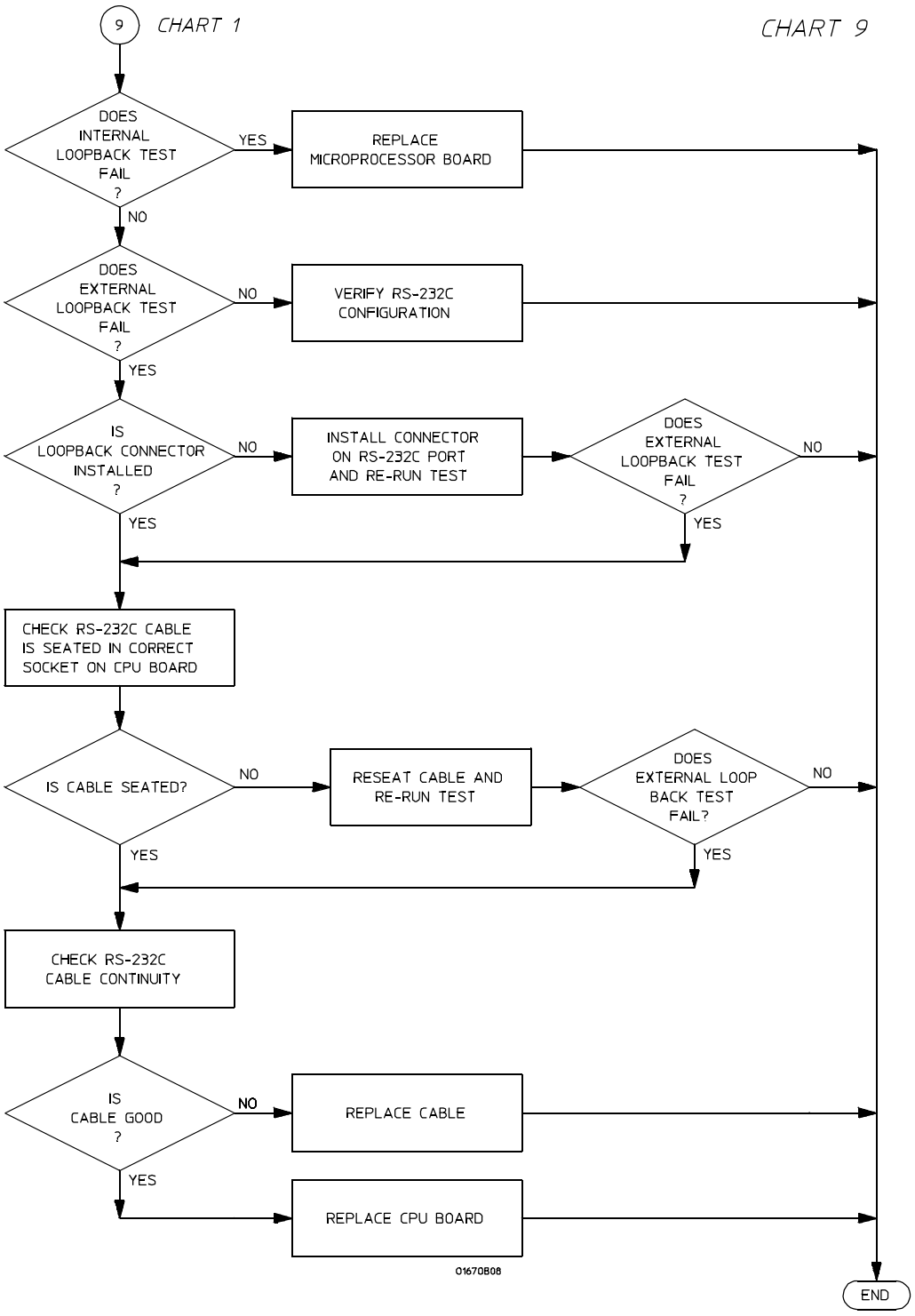
Troubleshooting Flowchart 5



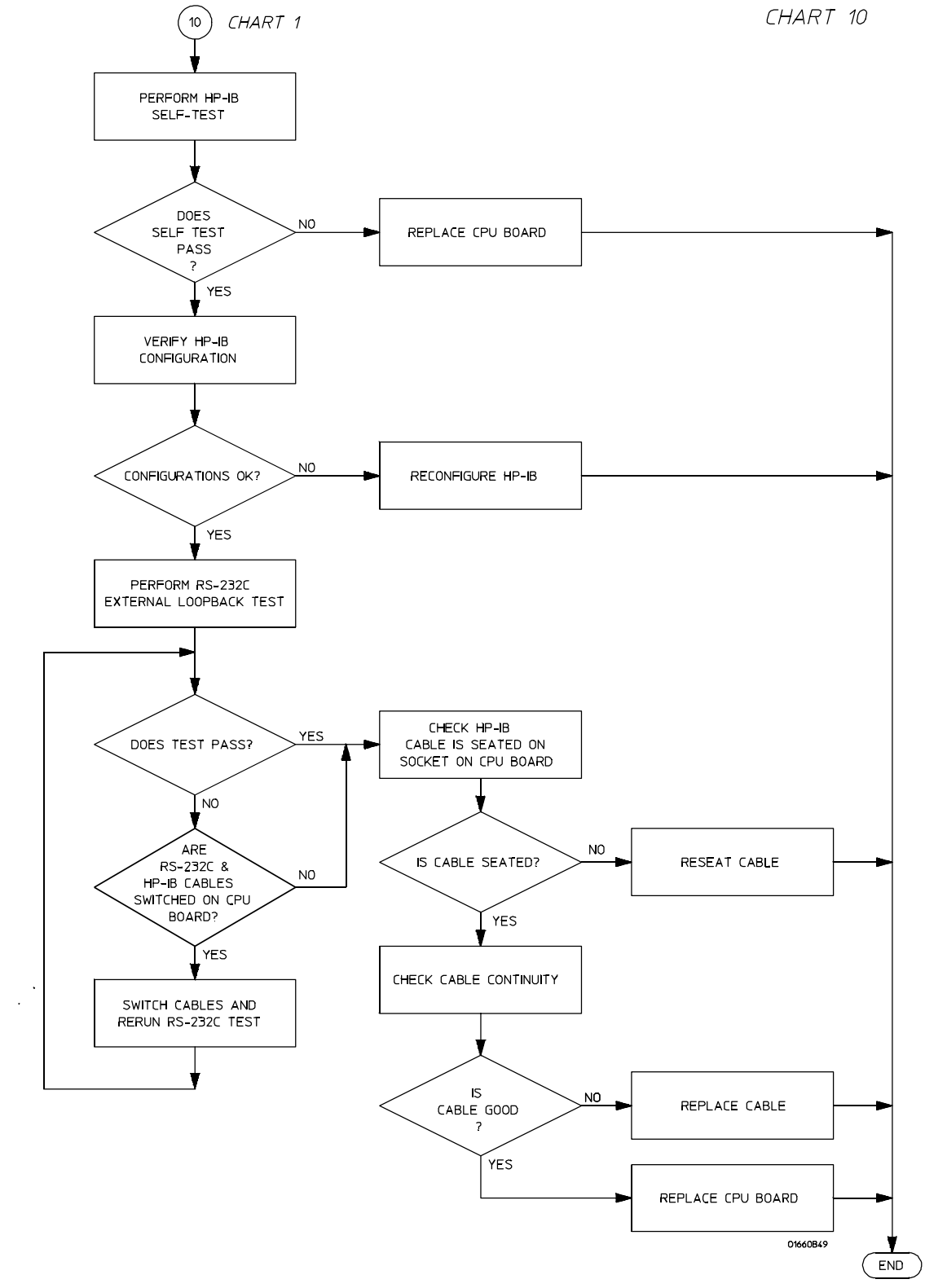
Troubleshooting Flowchart 6



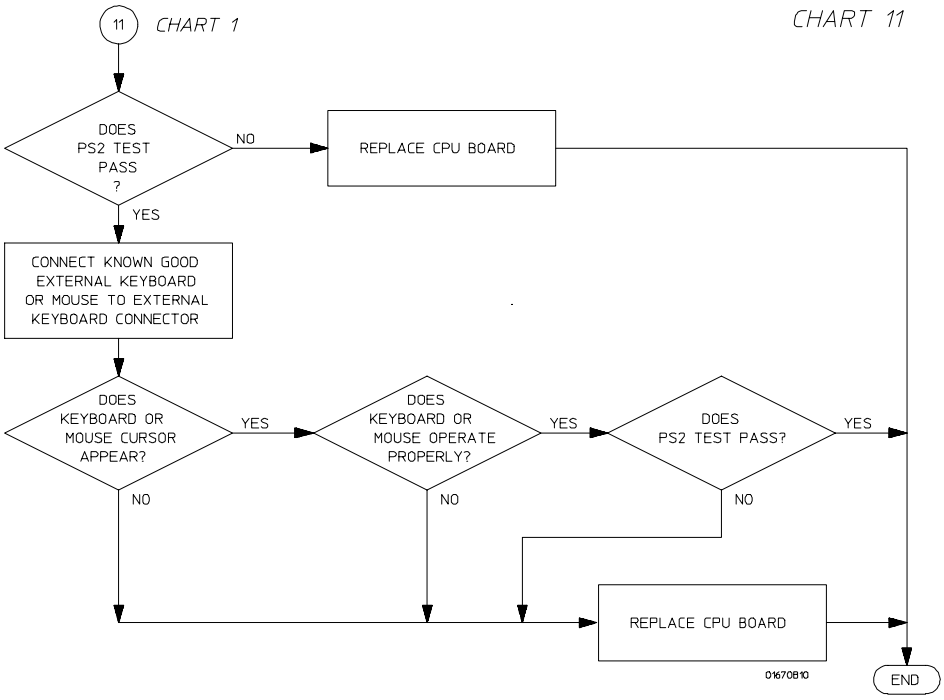
Troubleshooting Flowchart 7



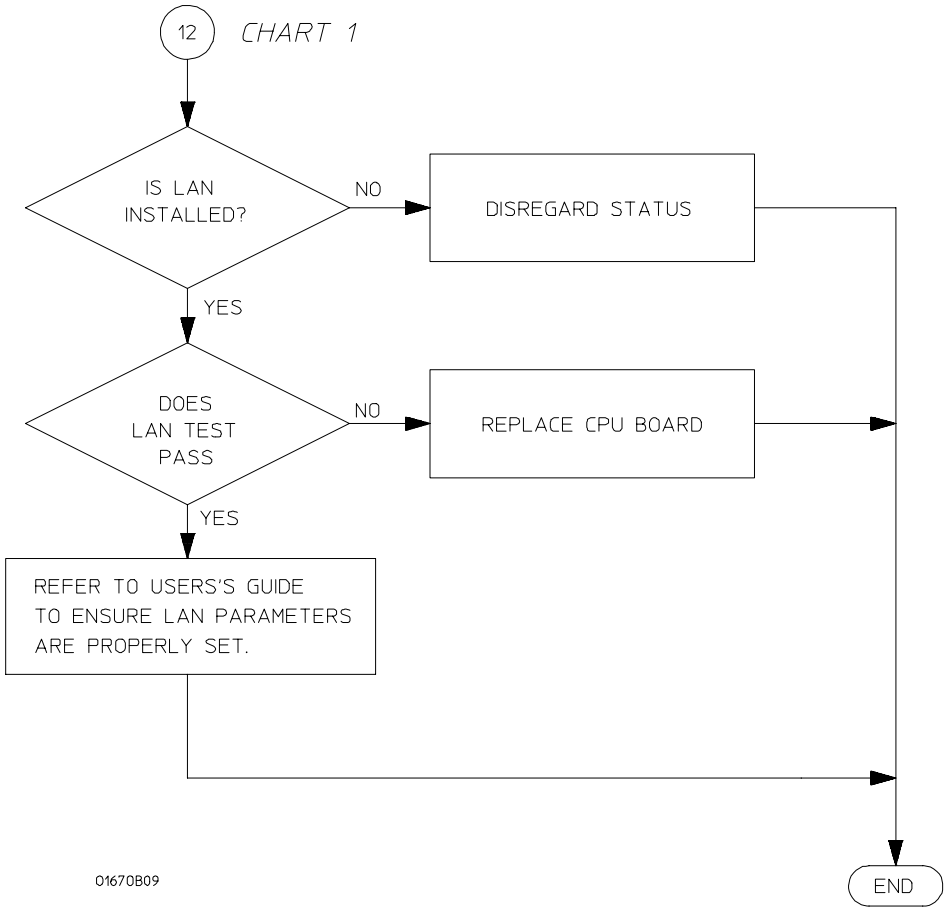
Troubleshooting Flowchart 9 (flowchart 8 deleted)



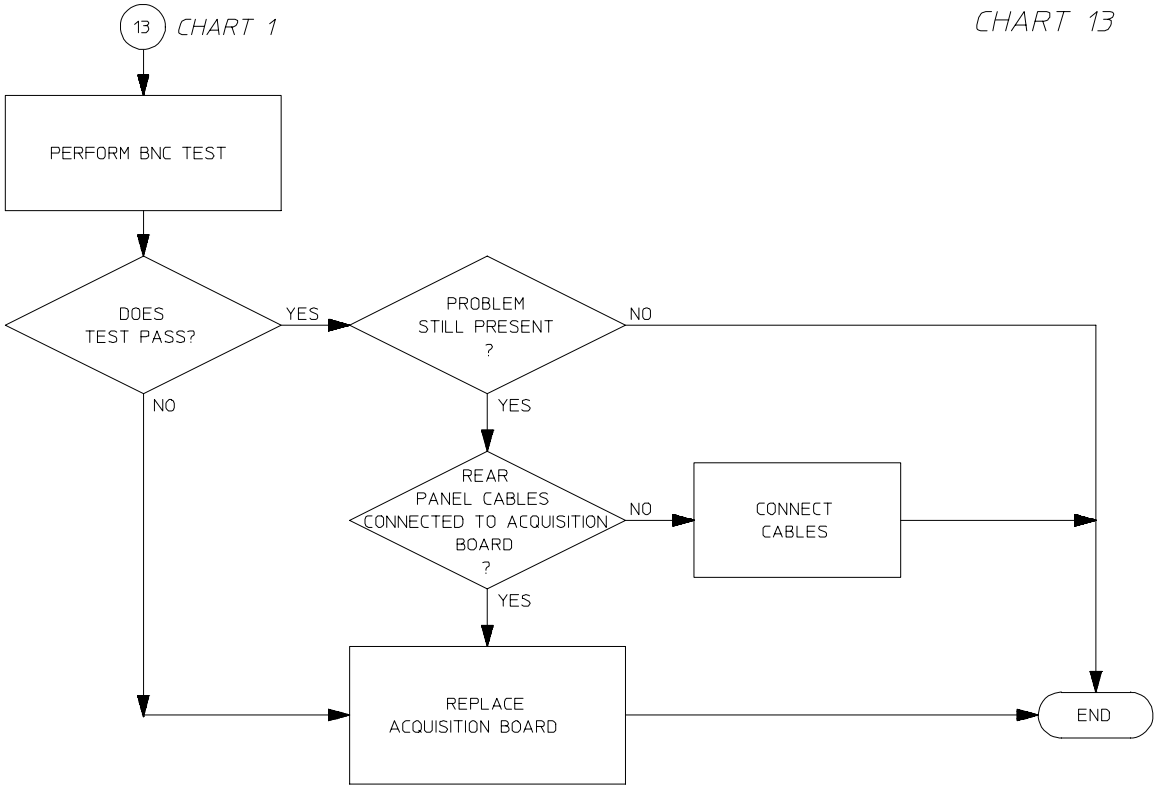
Troubleshooting Flowchart 10



Troubleshooting Flowchart 11



Troubleshooting Flowchart 12



Troubleshooting Flowchart 13

To check the power-up tests

The logic analyzer automatically performs power-up tests when you apply power to the instrument. The revision number of the operating system shows in the upper-right corner of the screen during these power-up tests. As each test completes, either "PASSED" or "FAILED" prints on the screen in front of the name of each test.

1. Disconnect all inputs, then insert a formatted disk into the disk drive.
2. Let the instrument warm up for a few minutes, then cycle power by turning off then turning on the power switch.

   If the instrument is not warmed up, the power-up test screen will complete before you can view the screen.
3. As the tests complete, check if they pass or fail.

   The Flexible Disk Test reports No Disk if a disk is not in the disk drive.

Performing Power-Up Self-Tests

passed	ROM text
passed	RAM test
passed	Interrupt test
passed	Display test
passed	PS2 Controller Test
passed	Hard Disk Test
No Disk	Flexible Disk Test

To run the self-tests

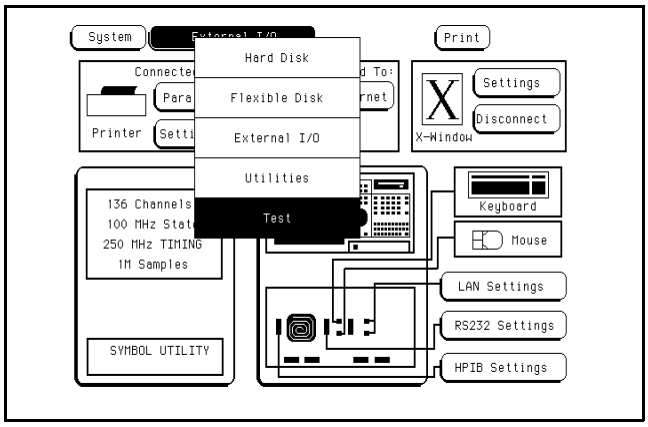
Self-tests identify the correct operation of major functional areas of the instrument. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the instrument.

These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

1 If you just did the power-up self-tests, go to step 2.

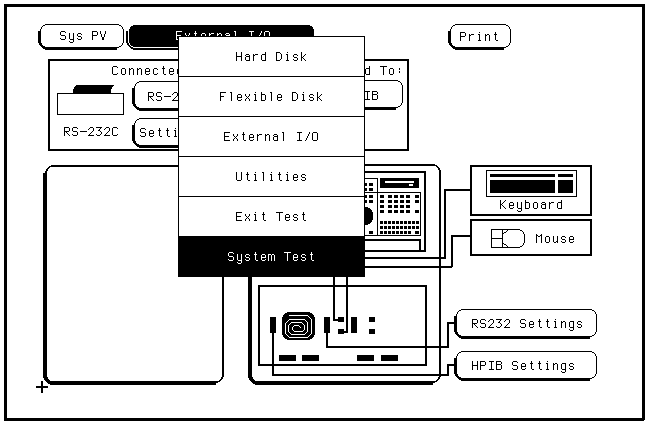
If you did not just do the power-up self-tests, disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.

2 Press the System key, then select the field next to System. Select Test in the pop-up menu.



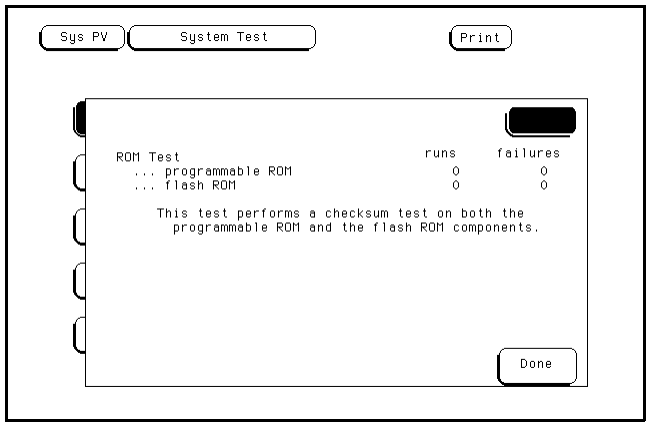
3 Select the box labeled Load Test System.

4 Press the System key, then select the field next to Sys PV. Select System Test to access the system tests.



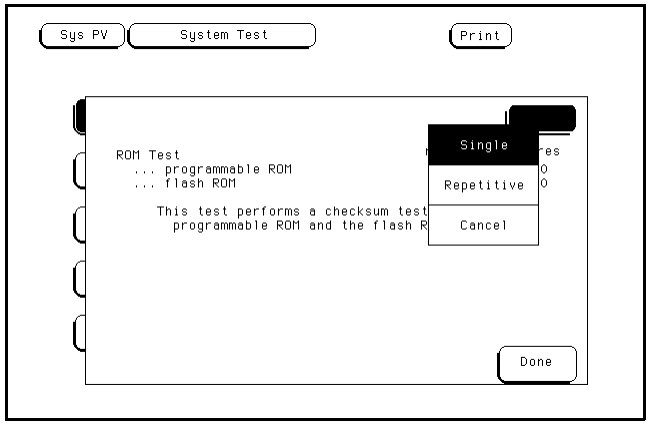
5 Select ROM Test. The ROM Test screen is displayed.

You can run all tests at one time by running All System Tests. To see more details about each test, you can run each test individually. This example shows how to run an individual test.

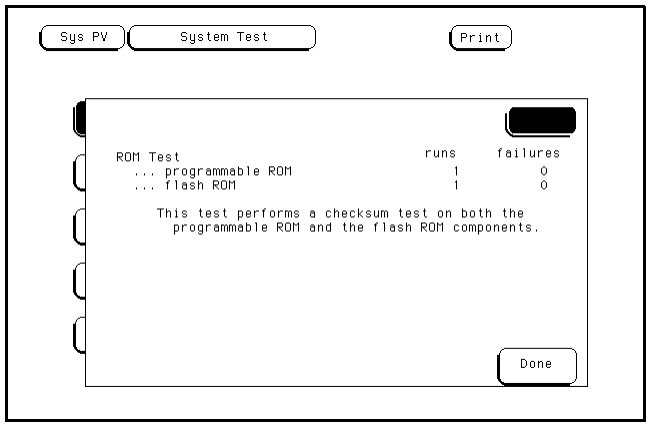


6 Select Run, then select Single.

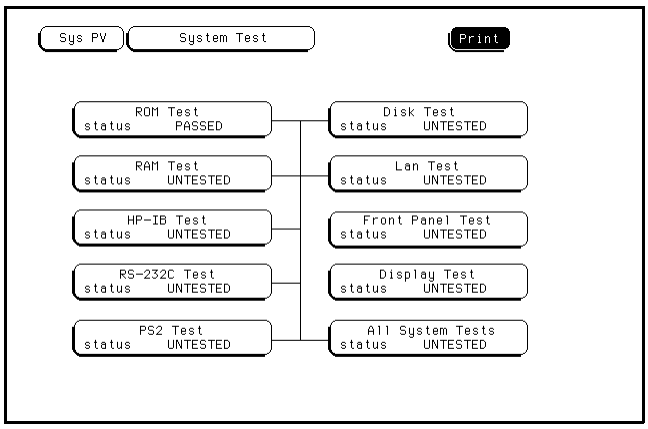
To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.



For a Single run, the test runs one time and the screen shows the results.



7 To exit the ROM Test, select Done. Note that the status changes to PASSED or FAILED.



8 Install a formatted disk that is not write protected into the flexible disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port. Run the remaining System Tests in the same manner.

9 Select the Front Panel Test.

A screen duplicating the front-panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color.

b Test the knob by turning it in both directions.

c Note any failures, then press the Done key a second time to exit the Front Panel Test. The test screen shows the Front Panel Test status changed to TESTED.

10 Select the Display Test.

A white grid pattern is displayed. These display screens can be used to adjust the display.

a Select Continue and the screen changes to full bright.

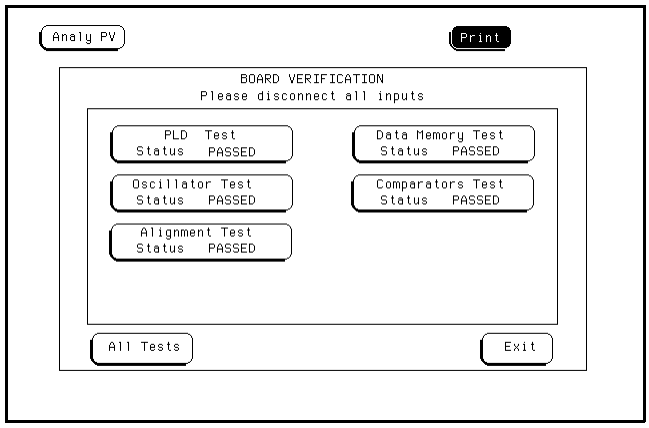
b Select Continue and the screen changes to half bright.

c Select Continue and the test screen shows the Display Test status changed to TESTED.

11 Select Sys PV, then select Analy PV in the pop-up menu. In the Analy PV menu, select Board Verification Tests. In the Board Verification menu, select All Tests.

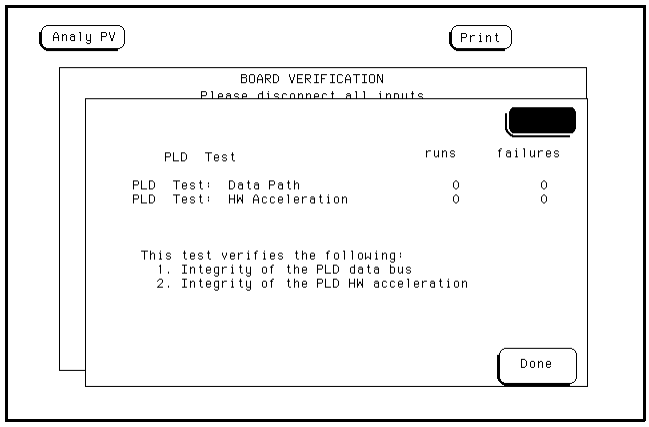
You can run all tests at one time by selecting All Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All Tests changes from UNTESTED to TESTED.



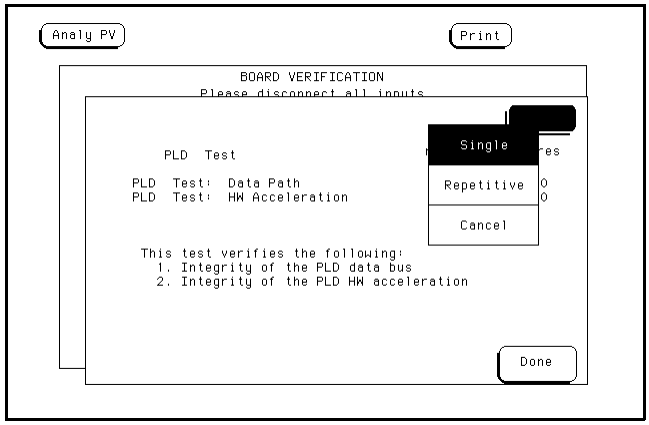
12 Select PLD Test. The PLD Test screen is displayed.

You can run all tests at one time by running All System Tests. To see more details about each test, you can run each test individually. This example shows how to run an individual test.

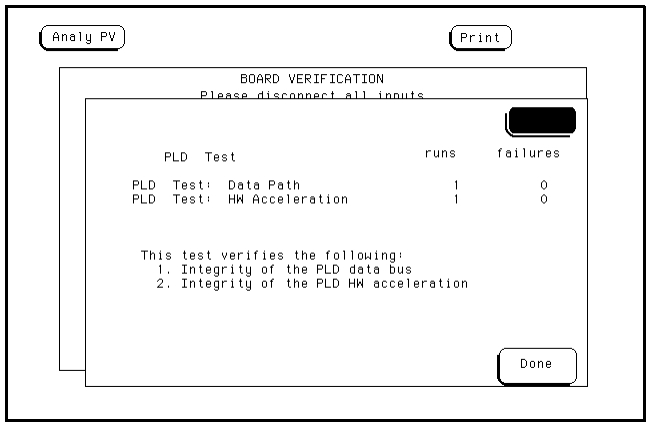


13 Select Run, then select Single.

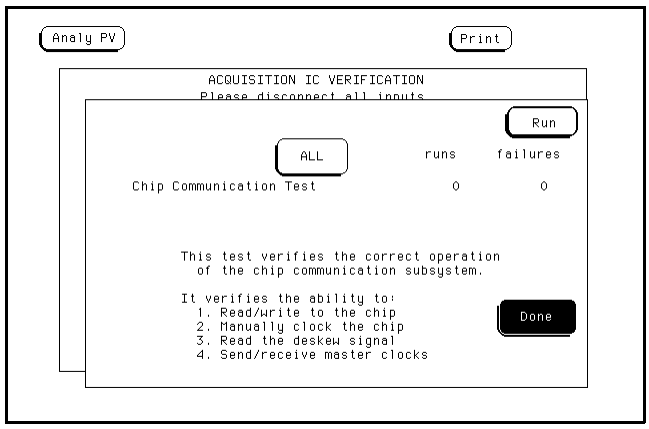
To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.



For a Single run, the test runs one time, and the screen shows the results.



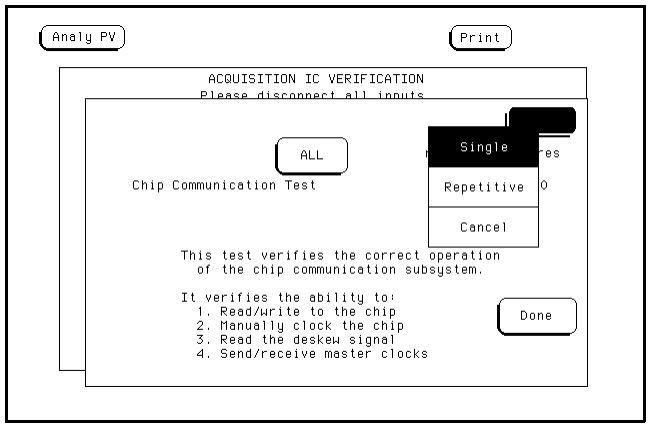
14 Select Exit to exit the Board Verification Test. In the Analy PV menu, select Acquisition IC Verification, then select Communication Test.



15 Select Run, then select Single.

To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.

For a Single run, the test runs one time and the screen shows the results.



To test the power supply voltages

To check the voltages, the power supply must be loaded by either the acquisition board or with an added resistor.

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

Hazardous voltages exist on the power supply, the CRT, and the CRT driver board. Only service-trained personnel who are aware of the hazards involved, such as fire and electrical shock, should perform this procedure.

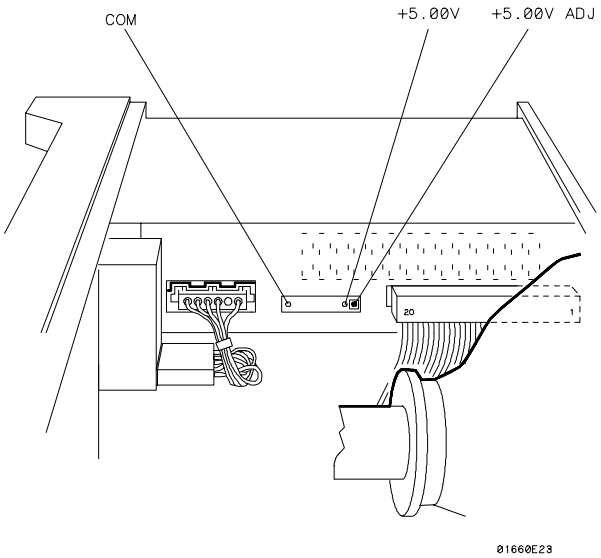
Loaded by the acquisition board

1. Turn off the instrument, then remove the power cable. Remove the cover of the instrument.
2. Connect the power plug, then turn on the instrument.
3. Check for the +5 V, as indicated by the figure below.

Loaded by the added resistor

1. Turn off the instrument, then remove the power cable. Remove the cover of the instrument and the disk drive assembly.
2. Remove the power supply far enough to disconnect the power supply cable from the acquisition board. Bring the end of the cable up and out of the instrument.

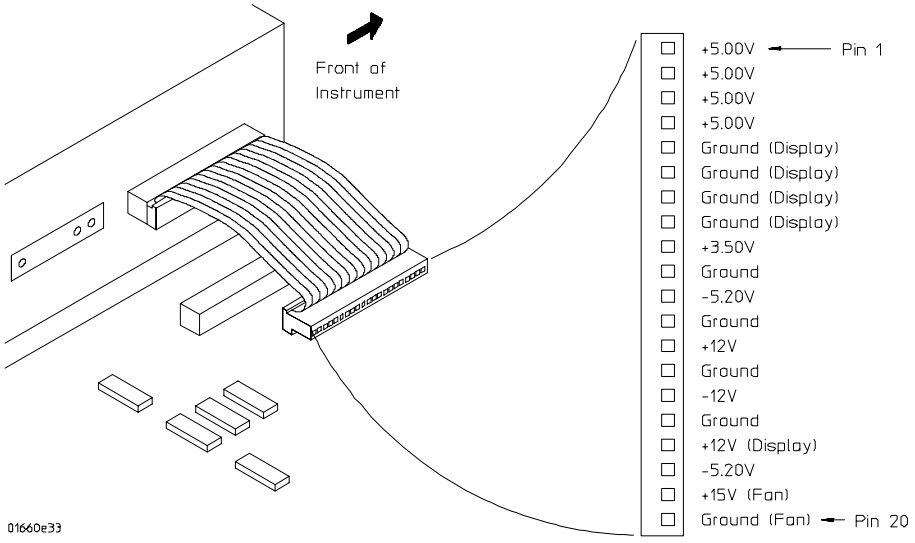
   Use the disconnected cable to load the supply and to make measurements.
3. Load the +5.00 V supply with a 2-Ω, 25-watt resistor.
   a. With a jumper wire, connect one end of the resistor to one of the 5.00V pins (pins 1 through 4) on the supply cable.
   b. With another jumper wire, connect the other end of the resistor to one of the ground pins (pins 5 through 7) on the supply cable.
4. Connect the power plug, then turn on the instrument.
5. Check for the +5 V as indicated by the figure below.



6 Check for the voltages on the power supply cable using the values in the following table.

Signals on the Power Supply Cable

Pin	Signal	Pin	Signal
1	+5.00 V	11	–5.20 V
2	+5.00 V	12	Ground
3	+5.00 V	13	+12 V
4	+5.00 V	14	Ground
5	Ground (Digital)	15	–12 V
6	Ground (Digital)	16	Ground
7	Ground (Digital)	17	+12 V (Display)
8	Ground (Display)	18	–5.20 V
9	+3.50 V	19	+15 V (Fan)
10	Ground	20	Ground (Fan)



To test the CRT monitor signals

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

Hazardous voltages exist on the power supply, the CRT, and the CRT driver board. Only service-trained personnel who are aware of the hazards involved, such as fire and electrical shock, should perform this procedure.

1. Remove the cover of the instrument.
2. Check the CRT monitor input cable for the signals and the power supplies listed in the table below. The cable is the wide ribbon cable connecting the monitor to the acquisition board.

CRT Monitor Cable Signals

Pin	Signal	Pin	Signal
1	NC	2	+12 V
3	Ground	4	Ground
5	+12 V	6	Ground
7	+12 V	8	Ground
9	+12 V	10	HSYNC
11	VSYNC	12	+12 V
13	Ground	14	Ground
15	Ground	16	Video
17	Ground	18	NC
19	Ground	20	NC

To test the keyboard signals

Refer to chapter 6, "Replacing Assemblies," for instructions to remove covers and assemblies.

WARNING

Hazardous voltages exist on the power supply, the CRT, and the CRT driver board. Only service-trained personnel who are aware of the hazards involved, such as fire and electrical shock, should perform this procedure.

1. Turn off the instrument and remove the power cable.
2. Without disconnecting the keyboard cable, follow the keyboard removal procedure to loosen the keyboard. Leave the keyboard in place in front of the instrument.
3. Reconnect the power cable, then turn on the instrument.
4. Run the PV Front Panel Test, pressing all of the keys.
5. If a random key is not operating, go to the next step.

   If a group of keys do not work, then check the keyboard voltages and signals.

Keyboard Connector Signals

Pin	Signal	Pin	Signal
1	Keyboard Return	13	Keyboard Scan
2	"	14	"
3	"	15	"
4	"	16	"
5	"	17	"
6	"	18	"
7	"	19	LED
8	"	20	+5 V
9	Keyboard Scan	21	Ground
10	"	22	Knob
11	"	23	Ground
12	"	24	Knob

6. Allow the keyboard assembly to fall forward from the front panel. Separate the elastomeric keypad and keyboard panel from the PC board.
7. Using a paper clip or screwdriver, short the PC board trace of the non-operating key and look for an appropriate response on the display.
8. If the display responds as though the key was pressed, replace the elastomeric keypad.

   If the display does not respond as though the key was pressed, replace the keyboard.
9. Check the RPG connector.

   The RPG connector has a TTL pulse on pins 22 and 24 when you turn the knob. Pin 20 of the connector is +5 V.

To test the flexible disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

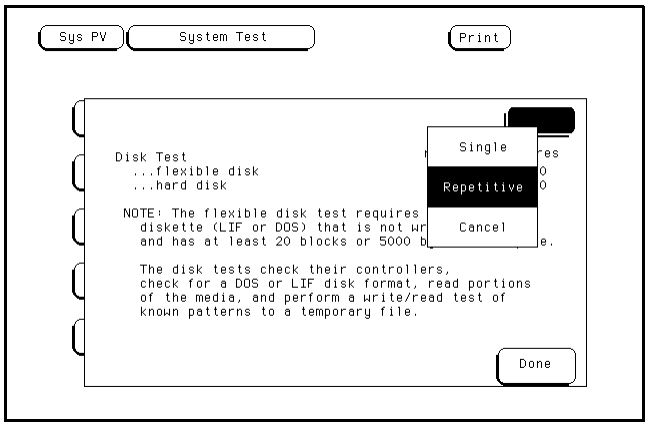
WARNING

This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	HP 54600B

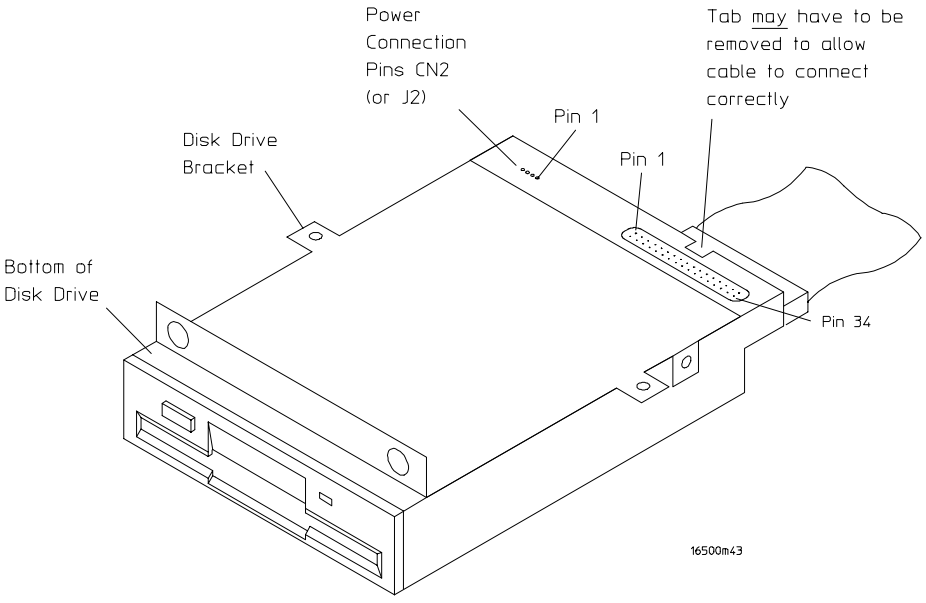
1. Turn off the instrument, then remove the power cable. Remove the instrument cover and the disk drive.
2. Reconnect the disk drive cable to the rear of the disk drive. Turn the disk drive over so that the solder connections of the cable socket are accessible.
3. Connect the power cable, then turn on the instrument.
4. Insert the disk that contains the functional performance verification software and enter the test operating system.
5. In the Sys PV menu select the Disk test. Insert a disk that has enough available bytes to run the test in the disk drive, then select Run-Repetitive.



6 Check for the following signals using an oscilloscope.

Flexible Disk Drive Signals

Pin	Signal Description	Pin	Signal Description
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	Ground	8	Index
9	Ground	10	Drive Select
11	Ground	12	Drive Select
13	Ground	14	NC
15	Ground	16	Motor On
17	Ground	18	Direction
19	Ground	20	Step
21	Ground	22	Write Data
23	Ground	24	Write Gate
25	Ground	26	Track 00
27	Ground	28	Write Protect
29	Ground	30	Read Data
31	Ground	32	Side Select
33	Ground	34	Disk Change



7 Select Stop, and turn off the logic analyzer. Remove the power cable.

The test will not immediately stop when Stop is selected; it will continue until the current iteration of the disk test is completed and then stop.

8 Disconnect the disk drive cable and re-install the disk drive in the logic analyzer.

9 Reconnect the disk drive cable and install the logic analyzer cover.

To test the hard disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

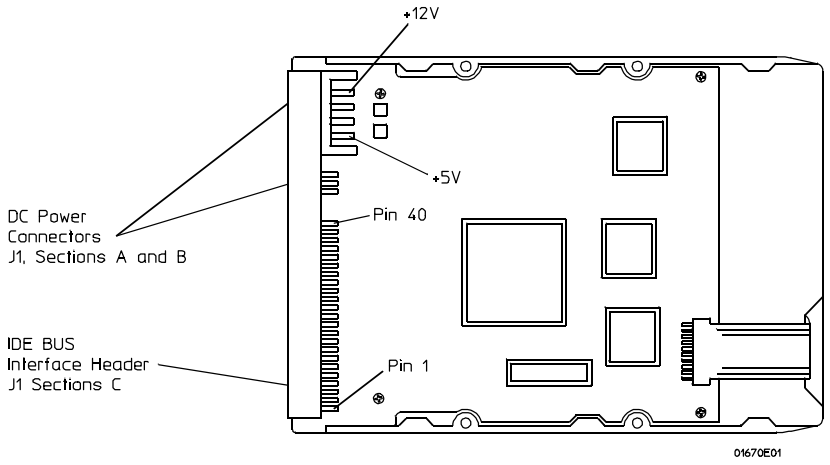
Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	HP 54600B

1. Turn off the instrument, then remove the power cable. Remove the instrument cover and the disk drive assembly.
2. Remove the hard disk drive from the disk drive assembly. Reconnect both hard disk drive cables to the rear of the disk drive. Turn the disk drive over so that the solder connections of the cable socket are accessible.
3. Connect the power cable, then turn on the instrument.
4. In the Sys PV menu select the Disk test. Select Run-Repetitive.
5. Check for the following signals using an oscilloscope.

Hard Disk Drive Signals

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	RESET	27	IORDY	34	PDIAG
3 - 18	DATA	28	CABLE SELECT	35	DAO
20	KEYPIN	29	DMACK	36	ADDR2
21	DMARQ	31	INTRQ	37	CS1FX
23	DIOW	32	IOCS16	38	CS3FX
25	DIOR	33	ADDR1	39	DASP

Pins 2, 19, 22, 24, 26, 30, 40 are GROUND



6 Select Stop, and turn off the logic analyzer. Remove the power cable.

The test will not immediately stop when you select Stop; it will continue until the current iteration of the disk test completes and then it stops.

7 Disconnect the disk drive cables. Re-install the hard disk drive onto the disk drive assembly, and then re-install the disk drive assembly in the logic analyzer.

8 Reconnect the disk drive cables and install the cover on the logic analyzer.

To perform the BNC test

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	100 MHz Bandwidth	HP 54600B
BNC Shorting Cap		1250-0074
BNC Cable		HP 10503A
BNC-Banana Adapter		1251-2277

1 Press the Config key.

2 Assign pods 1 and 2 to Machine 1.

To assign the pod field, select the pods 1 and 2 field, then select Machine 1 in the pop-up menu.

3 In the Analyzer 1 box, select the Type field. Select Timing in the pop-up menu.

4 Set up the trigger menu.

a Press the Trig key. Select Clear Trigger All.

b Select Arming Control. In the Arming Control pop-up menu, select the field labeled Run, then select Port In. Press the Done key.

5 Attach a BNC shorting cap to the External Trigger Input on the rear panel of the logic analyzer.

6 Using a BNC cable, connect the External Trigger output to the oscilloscope channel 1 input. Set the oscilloscope to Trigger On and measure TTL voltage levels.

7 Press the RUN front-panel key.

The warning "MACHINE 1 Waiting on level 1" will appear.

8 Remove the shorting cap from the rear-panel External Trigger input BNC.

9 The warning will go away and the oscilloscope will display a positive-going TTL pulse.

To test the logic analyzer probe cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8131A Option 020
Adapter (Qty 4)	SMA (m) - BNC (f)	HP 1250-1200
Coupler (Qty 4)	BNC (m)(m)	HP 1250-0216
6x2 Test Connectors (Qty 4)		

1 Turn on the equipment and the logic analyzer.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

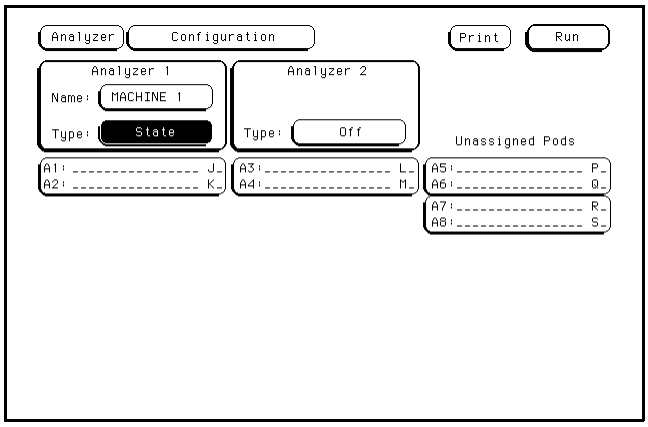
Channel 1	Channel 2	Period
Delay: 0 ps	Delay: 0 ps	100 ns
Dty: 50%	Dty: 50%	
High: 3.00 V	High: 3.00 V	
Low: 0.00 V	Low: 0.00 V	

b Enable the pulse generator channel 1 and channel 2 outputs (with the LEDs off).

3 Set up the logic analyzer Configuration menu.

a Press the Config key.

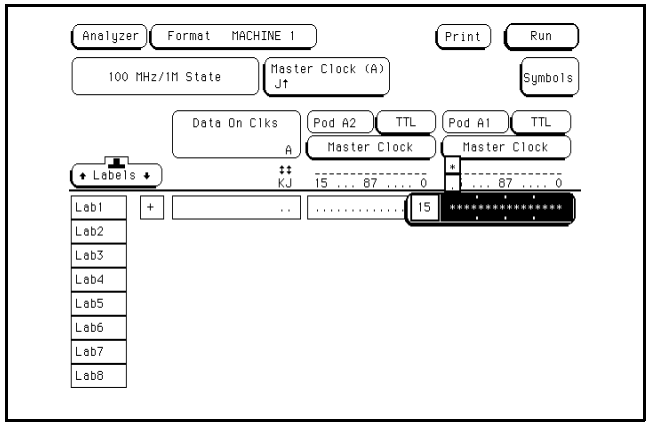
b In the Analyzer 1 box, select the field to the right of Type, then select State.



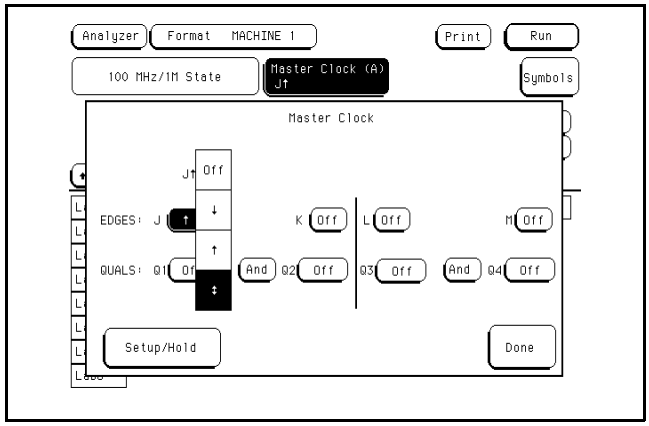
4 Set up the Format menu.

a Press the Format key.

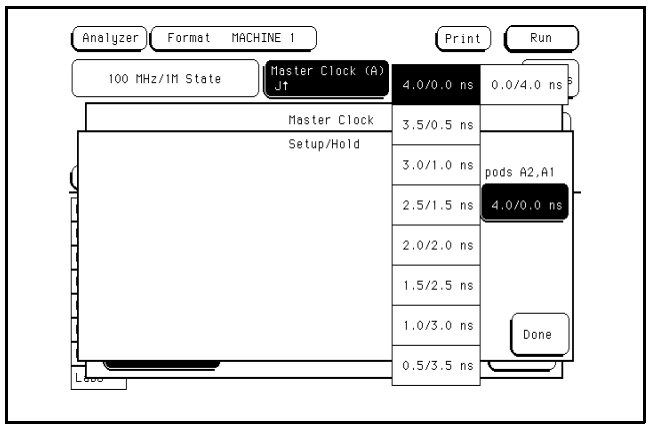
b Move the cursor to the field showing the channel assignments for the pod under test. Press the Clear Entry key until the pod channels are all assigned (all asterisks (*)). Press the Done key.



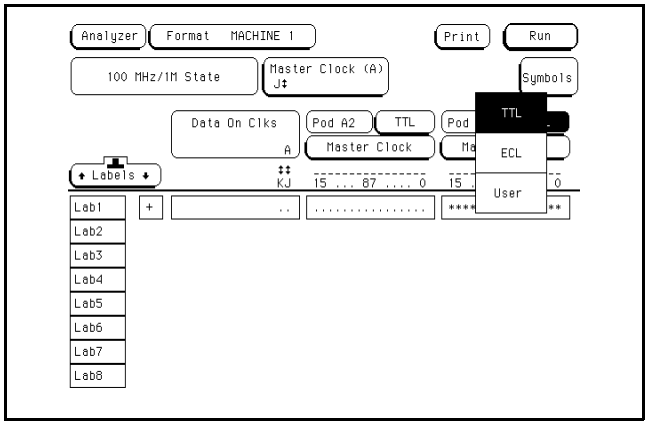
c Select Master Clock, then select a double edge for the clock of the pod under test. Turn off the other clocks.



d In the Master Clock menu, select Setup/Hold, then select 4.0/0.0 ns for the pod being tested. Select Done. Select Done again to exit the Master Clock menu.



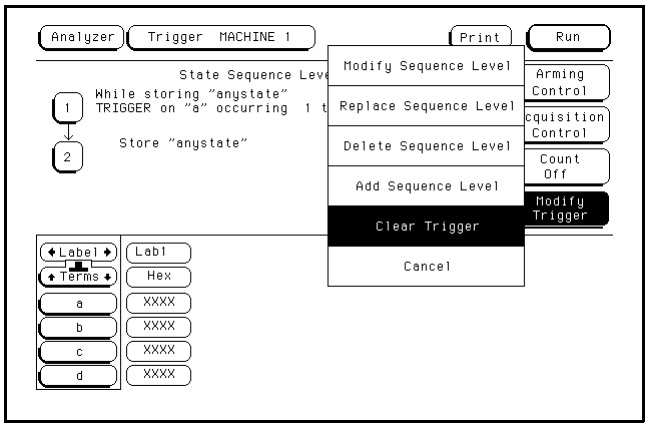
e Select the field to the right of the pod being tested, then select TTL.



5 Set up the Trigger menu.

a Press the Trigger key.

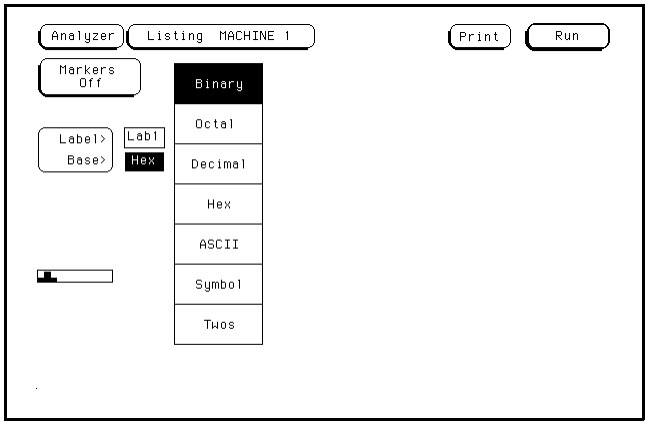
b Select Modify Trigger, then select Clear Trigger, then select All.



6 Set up the Listing menu.

a Press the List key.

b Select the field to the right of Base, then select Binary.



7 Using four 6-by-2 test connectors, four BNC Couplers, and four SMA (m) - BNC (f) Adapters, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, see chapter 3, "Testing Performance."

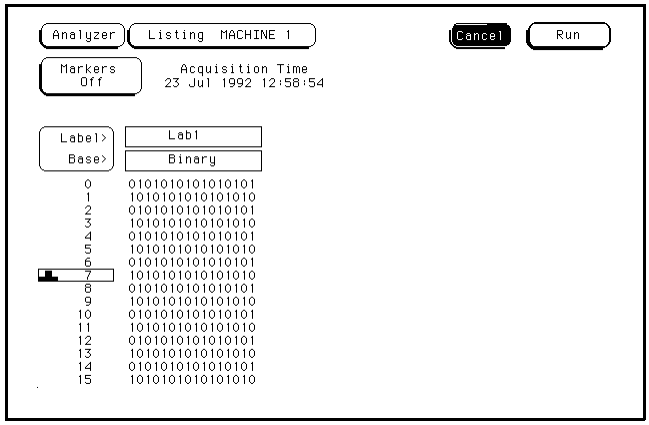
a Connect the even-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output and J-clock.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 $\overline{\text{Output}}$.

c Connect the even-numbered channels of the upper byte of the pod under test and the clock channel to the pulse generator channel 2 Output.

d Connect the odd-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 $\overline{\text{Output}}$.

8 On the logic analyzer, press Run. The display should look similar to the figure below.



9 If the display looks like the figure, then the cable passed the test.

If the display does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include the following:

- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

Return to Troubleshooting Flowchart 7.

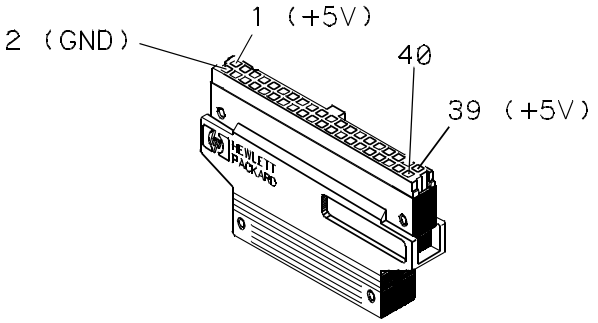
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection device. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	HP E2373A

- Use the multimeter to verify the +5 V on pins 1 and 39 of the probe cables.



MISC/EX50

6

Replacing Assemblies

Replacing Assemblies

This chapter contains the instructions for removing and replacing the assemblies of the logic analyzer. Also in this chapter are instructions for returning assemblies.

WARNING Hazardous voltages exist on the power supply, the CRT, and the CRT driver board. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors on the power supply board and the CRT driver board to discharge before servicing the instrument.

CAUTION Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Never attempt to remove or install any assembly with the instrument on or with the power cable connected.

Replacement Strategy

These replacement procedures are organized as if disassembling the complete instrument, from the first assembly to be removed to the last. Some procedures say to remove other assemblies of the instrument, but do not give complete instructions. Refer to the procedure for that specific assembly for the instructions. Use the exploded view of the instrument on the next page as a reference during the replacement procedures.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this logic analyzer.

Tools Required

#10 TORX screwdriver
#15 TORX screwdriver
#1 Posidrive screwdriver
3/16-inch (5-mm) nut driver
9/32-inch (7-mm) nut driver

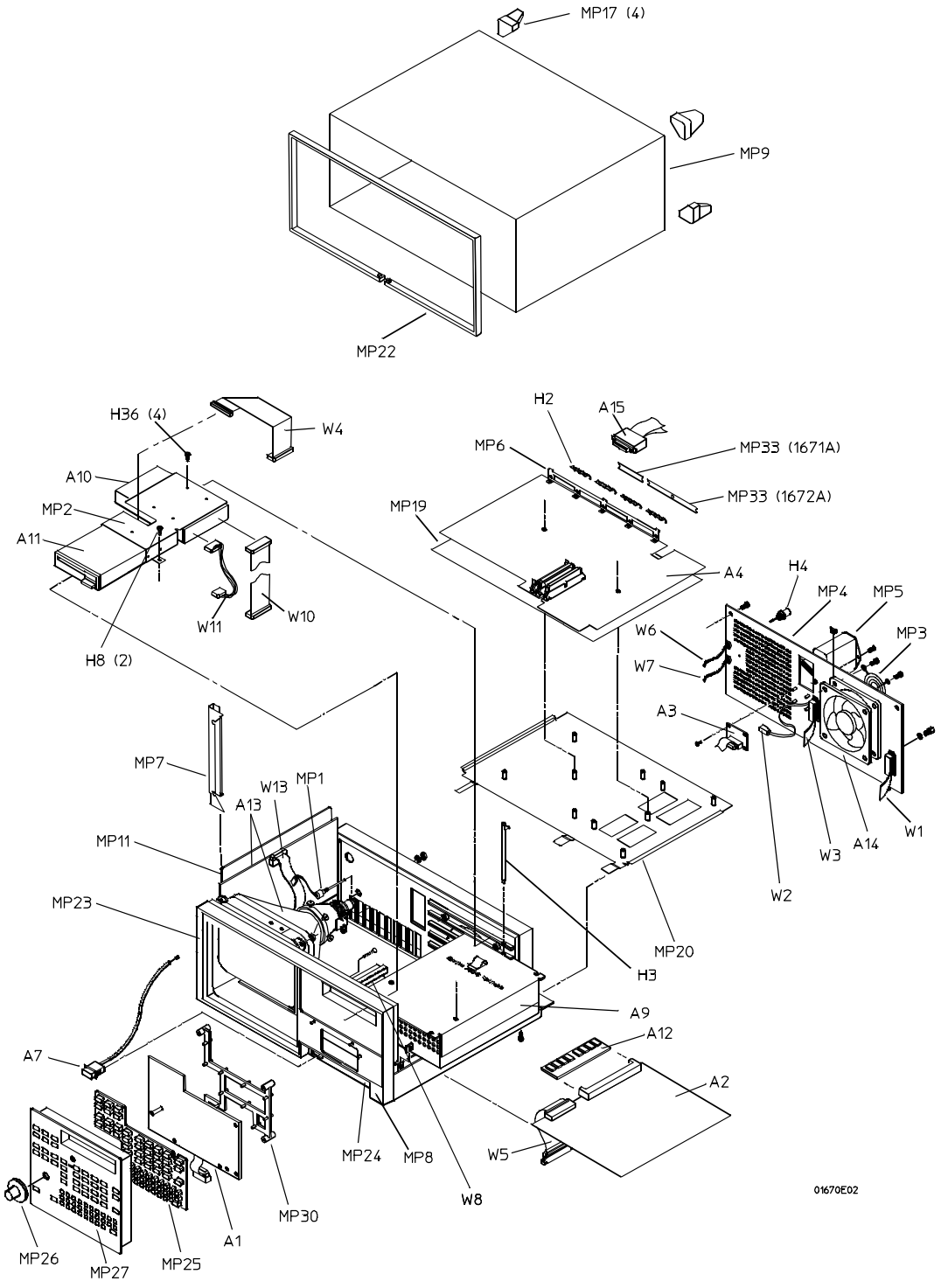
Exploded View

Listing

A1	Keyboard
A2	CPU board
A3	I/O Board
A4	Acquisition board
A7	Switch actuator
A9	Power supply
A10	Hard disk drive
A11	Flexible disk drive
A12	SIMM
A13	Monitor assembly
A14	Fan
H3	Locking pin
H4	BNC connector

MP1	Intensity adjustment
MP2	Disk drive bracket
MP3	Fan guard
MP4	Rear panel
MP5	Line filter
MP6	Ground bracket
MP7	Ground bracket
MP8	Cabinet
MP11	Handle plate
MP19	Insulator
MP20	Mounting plate
MP23	Label
MP24	Label
MP25	Elastomeric keypad
MP26	RPG knob
MP27	Keyboard panel
MP29	Front panel spacer
MP30	Keyboard spacer

W1	HP-IB cable
W2	Fan cable
W3	RS-232-C cable
W4	Flexible disk drive cable
W5	Cable-60 conductor
W6	Jumper cable-orange
W7	Jumper cable-white
W8	Power supply cable
W10	Hard disk drive data cable
W11	Hard disk drive power cable
W12	I/O Board Cable
W13	Sweep cables



Exploded View of the HP 1670D

To remove and replace the handle

- Remove the two screws in the endcaps, then lift off the handle.

To remove and replace the feet and tilt stand

1. Remove the screws connecting the four rear feet to the instrument.
2. Separate the rear feet from the instrument to remove them.
3. Press the locking tab on the bottom feet, then remove them.
4. Remove the tilt stand from the bottom front feet by lifting the stand up and out of the foot.
5. Reverse this procedure to install the feet and tilt stand.

To remove and replace the cover

1. Turn the power off and remove the power cord.
2. Remove the probe plate and disconnect the logic analyzer cables from the rear panel.
3. Using the previous procedures, remove the handle and the four rear feet.
4. Remove the seven screws from the front molding, then slide the molding forward to remove it.
5. Remove the cover.

   To remove the cover, set the instrument upright and facing toward you. Slide the chassis toward the front, out of the cover, and set it on a static-safe work area.
6. Reverse this procedure to install the cover.

   Check that all assemblies are properly installed before installing the cover.

   When installing the chassis in the cover, check that the tabs located at the bottom, rear of the cover align with the holes in the rear panel.

To remove and replace the disk drive assembly

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
2. Disconnect the two disk-drive ribbon cables from the rear of both disk drives. Peel the cables away from the double-sided tape used to secure the cables to the disk drive bracket.
3. Disconnect the power cable from the rear of the hard disk drive.
4. Remove the two screws that attach the disk drive bracket to the power supply.
5. Slide the disk drive assembly toward the front of the instrument about 1/2 inch (1.25 cm). Angle the rear of the bracket up and out of the chassis. Then remove the disk drive assembly completely out of the chassis by sliding the assembly toward the rear of the instrument.
6. To remove the flexible disk drive from the bracket, remove the four screws that attach the flexible drive to the bracket, two on each side.
7. To remove the hard disk drive, remove the four screws on top of the bracket that attach the hard drive to the bracket. If a new hard disk drive is being installed, then two rubber feet must be installed on the hard drive between the hard drive and the power supply.
8. Reverse this procedure to install the disk drive assembly.

   Check that the following assemblies are properly installed before installing the disk drive:
   - Monitor
   - Front Panel
   - Switch Actuator
   - CPU Board
   - Power Supply

To remove and replace the power supply

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before continuing.

2 Lift the PCB locking pins out of the chassis.

3 Slide the power supply out far enough to reach the power supply cables, then disconnect them from the power supply.

4 Slide the power supply the rest of the way out the side of the instrument.

5 Reverse this procedure to install the power supply.

Check that the following assemblies are properly installed before installing the power supply:

- Monitor
- Front Panel
- Switch Actuator
- CPU Board

To remove and replace the CPU board

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply

2 Disconnect the CPU board interface cable from the acquisition board by pressing down on the cable release tabs on the cable socket located on the acquisition board.

3 Disconnect the HP-IB and RS-232-C cables from the CPU board.

4 Disconnect the front panel cable from the CPU board.

5 Disconnect the I/O board cable from the CPU board.

6 Slide the board out the side of the instrument.

7 Reverse this procedure to install the CPU board.

Check that the following assemblies are properly installed before installing the CPU board:

- Monitor
- Front Panel
- Switch Actuator

To remove and replace SIMM memory

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- CPU Board

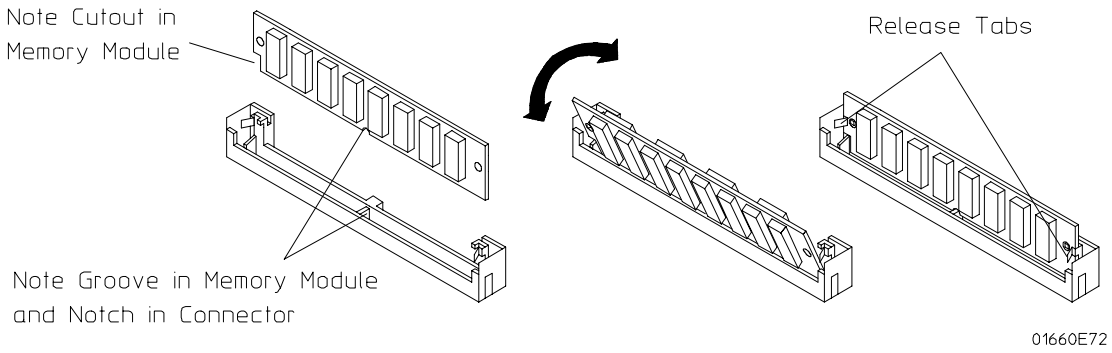
WARNING

Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before servicing the instrument.

2 Hold the release tabs away from the SIMM (single inline memory module), then pull the module out.

3 Reverse this procedure to install a replacement SIMM.

Slide the SIMM module into the connector at an angle, then push it down parallel to the CPU board.



To remove and replace the switch actuator assembly

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- CPU Board

2 Make sure the power switch is in the off position.

3 Disconnect the switch actuator from the line filter.

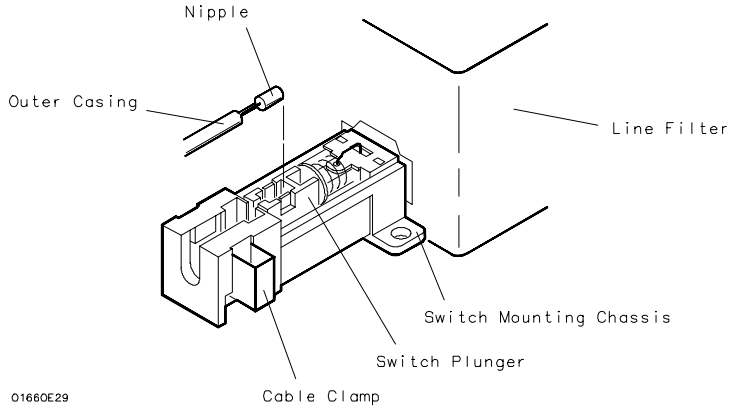
a Slide the clamp off of the outer casing far enough to release the switch actuator assembly.

CAUTION

If the wire in the switch actuator is bent, the complete assembly must be replaced. Refer to chapter 5, "Replaceable Parts," for the part number.

b Without bending the wire, gently pry the nipple out of the switch plunger.

c Slide the cable out of the switch assembly.



4 Remove the switch actuator assembly from the front of the cabinet.

To remove, depress the retaining ears on both sides of the assembly next to the front panel and push the assembly out the front.

5 Install the new switch actuator assembly. Make sure that the line filter switch is in the off position.

a Route the cable through the front panel, then snap the pushbutton into the front panel.

b Snap the nipple into the switch plunger.

c Position the free end of the outer casing into the switch mounting chassis. The edge of the outer casing should be all the way against the inner edge of the switch mounting chassis.

d Close the clamp by pushing it into the switch assembly until the clamp is seated.

6 Verify the push-on, push-off action of the assembly.

To remove and replace the rear panel

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
2. Remove the switch actuator cable from the line filter according to "To remove and replace the switch actuator assembly."
3. Disconnect the BNC In/Out and fan cables on the acquisition board.
4. Disconnect the RS-232-C and HP-IB cables from the CPU board.
5. Disconnect the I/O cable from the I/O board on the rear panel.
6. Remove the six rear panel screws.
7. Lift the rear panel away from the chassis.
8. Reverse this procedure to install the rear panel.

   Check that the following assemblies are properly installed before installing the rear panel:
   - Monitor
   - Acquisition Board

   When installing the rear panel, check that the alignment tabs on the acquisition board are lined up with the corresponding holes in the rear panel.

To remove and replace the acquisition board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Disconnect the sweep cable from acquisition board.
3. Disconnect the CPU board interface cable by pressing down on the cable release tabs on the cable socket located on the board.
4. Disconnect the power supply cable.
5. Slide the mounting plate out the rear of the instrument.

   Verify that the cable release tabs are down to slide the mounting plate out, then slide the mounting plate toward the rear out of the chassis.
6. Separate the acquisition board from the mounting plate by removing all screws attaching the board to the mounting plate.
7. Reverse this procedure to install the acquisition board.

   Check that the monitor is properly installed before installing the acquisition board

   When installing the mounting plate, check that the alignment tabs on the mounting plate are installed in the alignment holes in the inside bottom, front of the chassis.

To remove and replace the front panel and keyboard

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - CPU Board
2. Remove the four screws connecting the front panel.
3. Slide the front panel assembly out the front of the instrument.
4. Slide the spacers out the front of the instrument to remove them.

   Be careful not to lose the copper ground strips on the spacer.

   When installing the spacer, insert the pins of the spacer in the appropriate holes in the chassis. You can hold the spacer in place while installing the front panel by holding it with your finger through the disk drive mounting slot in the chassis.
5. Remove the RPG knob by pulling the knob off the RPG shaft.
6. Disassemble the front panel assembly by lifting the keyboard circuit board away from the front panel.
7. Lift the elastomeric keypad out of the front panel.
8. Reverse this procedure to assemble and install the front panel assembly.

   When assembling the front panel, check that the holes in the elastomeric keypad and the keyboard circuit board align with the pins on the front panel.

To remove and replace the intensity adjustment

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Disconnect the intensity adjustment cable from the CRT driver board.
3. Using a nut driver, remove the hex nut attaching the intensity adjustment to the chassis.
4. Slide the intensity adjustment assembly toward the front and up out of the instrument.
5. Reverse this procedure to install the intensity adjustment.

   When installing the intensity adjustment, check that the keying tab on the adjustment aligns with the keying hole in the chassis.

To remove and replace the monitor

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- CPU Board
- Rear Panel
- Acquisition Board
- Intensity Adjustment

WARNING Hazardous voltages exist on the CRT and the CRT driver board. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before servicing the instrument.

2 Disconnect the cable from the rear of the CRT.

3 Disconnect the yoke cable from the CRT driver board.

4 Disconnect the high voltage lead from the bell of the CRT.

5 Slide the CRT driver board up out of the chassis.

6 Using a nut driver, remove the three hex nuts attaching the monitor and ground bracket to the chassis, then remove the screw.

7 Slide the monitor assembly and ground bracket to the rear and up out of the chassis.

8 Reverse this procedure to install the monitor.

When installing the CRT driver board, check that the board is properly inserted in the circuit board tracks.

To remove and replace the handle plate

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover

2 Remove the four screens that attach the handle plate to the chassis.

3 Remove the handle plate.

To remove the handle plate, align the plate toward the front of the instrument, then move it up and out of the instrument.

4 Reverse this procedure to install the handle plate.

To remove and replace the fan

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- Rear Panel

2 Remove the four fan screws.

3 Lift the fan away from the rear panel.

4 Lift the fan guard away from the rear panel.

5 Reverse this procedure to install the fan.

When installing the fan, verify the correct orientation of the fan. If you mount the fan backwards, the instrument will overheat. Also, check the correct polarity of the fan cable.

To remove and replace the line filter

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- Rear Panel

2 Unsolder the ground wire from the lug on the rear panel.

3 Disconnect the line filter cable from the power supply.

4 Remove the two screws attaching the line filter to the rear panel.

5 Slide the line filter assembly out toward the rear.

6 Reverse this procedure to install the line filter.

To remove and replace the HP-IB and RS-232-C cables

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Remove the two hex standoffs connecting the HP-IB cable, then slide the HP-IB cable forward and out of the rear panel.
3. Remove the two hex standoffs connecting the RS-232-C cable, then slide the RS-232-C cable forward and out of the rear panel.
4. Reverse this procedure to install the HP-IB and RS-232-C cables.

To remove and replace the I/O board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Remove two jackscrews that attach the parallel printer (Centronics) port to the rear panel.
3. Remove four screws that secure the I/O board to the rear panel.
4. Reverse this procedure to install the I/O board onto the rear panel.

To return assemblies

Before shipping the logic analyzer or assemblies to Hewlett-Packard, contact your nearest Hewlett-Packard Sales Office for additional details.

1. **Write the following information on a tag and attach it to the part to be returned.**
   - Name and address of owner
   - Model number
   - Serial number
   - Description of service required or failure indications
2. **Remove accessories from the logic analyzer.**

   Only return accessories to Hewlett-Packard if they are associated with the failure symptoms.
3. **Package the logic analyzer.**

   You can use either the original shipping containers, or order materials from an HP Sales Office.

CAUTION For protection against electrostatic discharge, package the logic analyzer in electrostatic material.

4. **Seal the shipping container securely, and mark it FRAGILE.**

7

Replaceable Parts

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your logic analyzer.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Hewlett-Packard Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Hewlett-Packard Sales Office.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the HP Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Hewlett-Packard Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and there are no invoices.

For Hewlett-Packard to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Hewlett-Packard Sales Office. Addresses and telephone numbers are located in a separate document at the back of the service guide.

Exchange Assemblies

Some assemblies are part of an exchange program with Hewlett-Packard.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Hewlett-Packard.

After you receive the exchange assembly, return the defective assembly to Hewlett-Packard. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Hewlett-Packard will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Hewlett-Packard Sales Office for information.

See Also "To return assemblies," in chapter 6.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

The exploded view does not show all of the parts in the replaceable parts list.

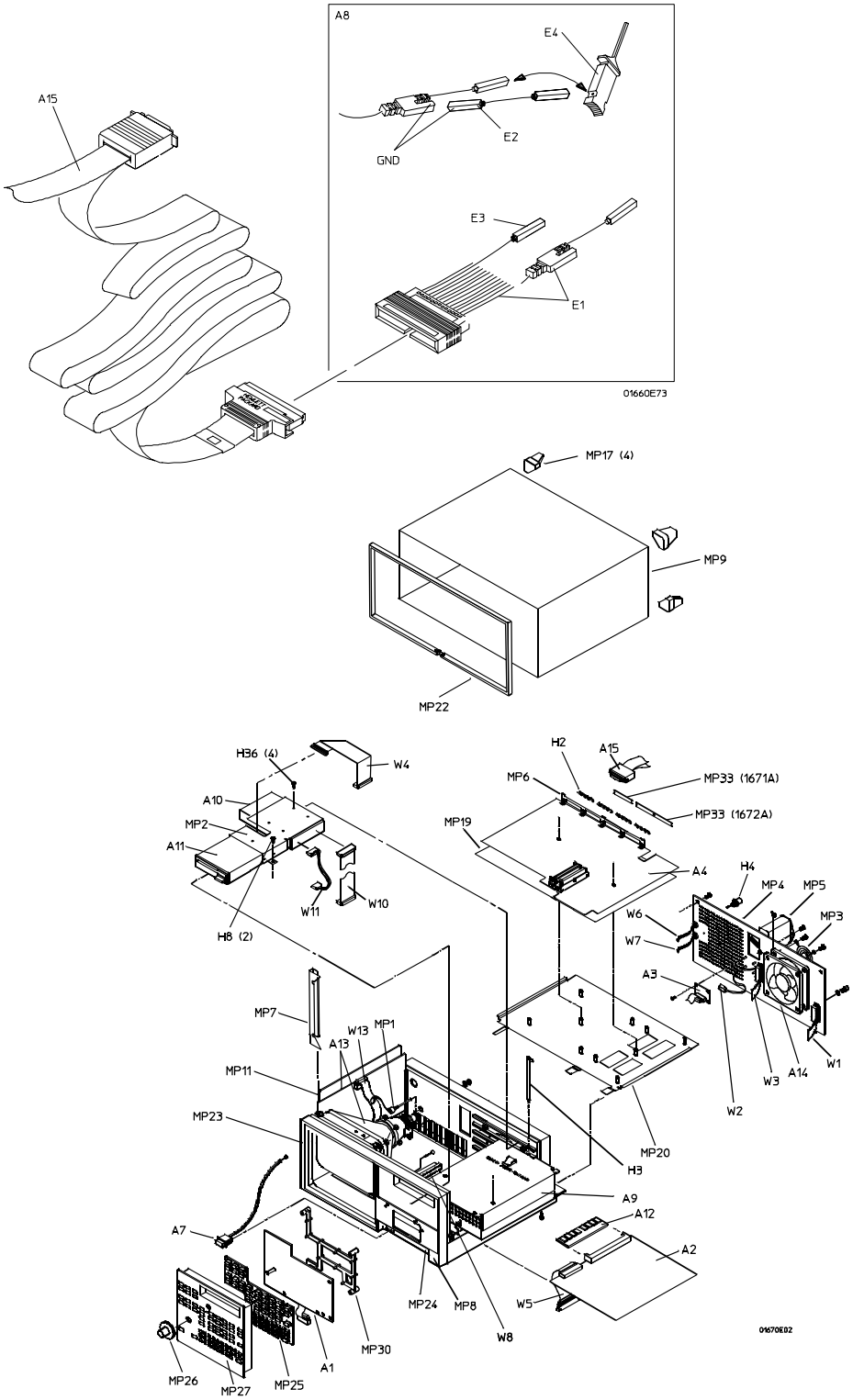
Information included for each part on the list consists of the following:

- Reference designator
- Hewlett-Packard part number
- Total quantity included with the instrument (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- E Miscellaneous Electrical Part
- F Fuse
- H Hardware
- MP Mechanical Part
- W Cable

Exploded View



Exploded view of the HP 1670D logic analyzer.

HP 1670-Series Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
			Exchange Board Assembly
	01660-69514		Exchange Board Assembly - CPU
	01670-69507		Exchange Board Assembly-ACQ 128 CH x 64K (HP 1670D)
	01670-69510		Exchange Board Assembly-ACQ 128 CH x 1024K (HP 1670D, opt 030)
	01670-69508		Exchange Board Assembly-ACQ 96 CH x 64K (HP 1671D)
	01670-69511		Exchange Board Assembly-ACQ 96 CH x 1024K (HP 1671D, opt 030)
	01670-69509		Exchange Board Assembly-ACQ 64 CH x 64K (HP 1672D)
	01670-69512		Exchange Board Assembly-ACQ 64 CH x 1024K (HP 1672D, opt 030)
			Replacement Parts
A1	01660-66502	1	Board assembly-keyboard
A2	01660-66514	1	Board assembly - CPU
A3	01660-66516	1	Board assembly - IO
A4	01660-66507	1	Board assembly-ACQ 128 CH x 64K (HP 1670D)
A4	01660-66510	1	Board assembly-ACQ 128 CH x 1024K (HP 1670D, opt 030)
A4	01660-66508	1	Board assembly-ACQ 96 CH x 64K (HP 1671D)
A4	01660-66511	1	Board assembly-ACQ 96 CH x 1024K (HP 1671D, opt 030)
A4	01660-66509	1	Board assembly-ACQ 64 CH x 64K (HP 1672D)
A4	01660-66512	1	Board assembly-ACQ 64 CH x 1024K (HP 1672D, opt 030)
A7	01660-61901	1	Switch Actuator
A8	01650-61608	4	Probe tip assembly (HP 1670D)
A8	01650-61608	3	Probe tip assembly (HP 1671D)
A8	01650-61608	2	Probe tip assembly (HP 1672D)
A9	0950-2261	1	Power supply
A10	0950-2740	1	Hard disk drive
A11	5042-1713	1	Flexible disk drive
A12	1818-5624	1	1024KX32 SIMM
A13	2090-0304	1	Monitor Assembly
A14	3160-1013	1	Fan-tubeaxial
A15	01660-61605	4	Probe cable (HP 1670D)
A15	16555-61606	4	Probe cable, shielded (HP 1670D, opt 030)
A15	01660-61605	3	Probe cable (HP 1671D)
A15	16555-61606	3	Probe cable, shielded (HP 1671D, opt 030)
A15	01660-61605	2	Probe cable (HP 1672D)
A15	16555-61606	2	Probe cable, shielded (HP 1672D, opt 030)
A16	A2839B	1	Mouse
E1	5959-9333		Replacement probe leads (5 per package)
E2	5959-9334		Replacement probe grounds (5 per package)
E3	5959-9335		Replacement pod ground (2 per package)
E4	5090-4356		Grabber kit assembly (20 grabbers per package)
F1	2100-0003	1	Fuse, 250V, 3A, non-time delay
H1	1400-0611	1	Clamp-cable
H2	01660-09101	4	Ground spring (HP 1670D)
H2	01660-09101	3	Ground spring (HP 1671D)
H2	01660-09101	2	Ground spring (HP 1672D)
H3	01650-46101	2	Locking pin PCB
H4	01660-67601	2	BNC connector assembly
H8	0515-1363	10	MS 3.0 5 TH T10 (flexible disk drive, disk drive assembly, handle plate)
H10	0515-0430	12	MS M3 .0X0 .5X6MM PH T10 (acquisition board, rear panel to chassis, I/O board to rear panel)
H11	0515-2349	5	MS M3.0 X 0.50 - 14MM LG (trim strip cover to cabinet)
H12	0515-1035	2	MSFH M3 8 T10 (line filter)
H13	0515-1103	2	MSFH M3 10 T10 (trim strip cover to cabinet)
H14	0515-0664	4	MSPH M3 12 SMS10 (rear feet to cabinet)
H15	2950-0072	1	NUTH 1/4-32 .062 (intensity adjustment)
H16	2950-0001	2	NUTH 3/8-32 .093 (BNC trigger ports)
H17	0535-0056	3	NUT-HEX (monitor assembly)
H20	0515-0382	3	SM assembly M4 X 0.7 12MM-LG (monitor assembly, handle)
H21	0515-1349	4	SM M3 X 0.5 30MM-LG (front panel assembly)
H22	0380-1482	2	STDF-HEX .34-IN (HP-IB cable)
H23	3050-0010	4	WFL.147 .312 .03 (rear feet)
H24	2190-0009	2	WIL.168 .340 .02 (HP-IB cable)
H25	2190-0027	1	WIL.256 .478 .02 (intensity adjustment)
H26	2190-0016	2	WIL.377 .507 .02 (BNC connectors)
H28	0515-1031	4	MSF M3 6 T10 (accessory pouch)

HP 1670-Series Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
H34	0403-0179	2	Bumper-adhesive back (hard disk drive)
H35	0380-1858	4	Jackscrew with lock (RS-232, Centronics port to rear panel)
H36	2360-0462	4	MSPH 6-32 .25 in. (hard disk drive)
H37	0515-2306	6	MSPH M3.0 x 0.50 10 mm (probe cable to rear panel)
MP1	01660-61606	1	Intensity adjustment assembly
MP2	01660-01208	1	Bracket-disk drive
MP3	3160-0092	1	Fan guard
MP4	01670-00201	1	Rear panel
MP5	54501-62702	1	Line filter assembly
MP6	01660-01205	1	Ground bracket
MP7	01650-01202	1	Ground bracket
MP8	01660-60001	1	Cabinet assembly
MP9	01660-04102	1	Cover assembly
MP10	01660-44901	1	Handle vinyl grip
MP11	01660-01202	1	Handle plate
MP13	35672-21703	2	Strap retainer
MP14	35672-45004	2	Handle end cap
MP15	5041-8801	2	Foot
MP16	1460-1345	2	Tilt stand
MP17	01660-40501	4	Rear foot
MP18	5041-8822	2	Non-skid foot
MP19	01660-45401	1	Circuit board insulator
MP20	01660-01201	1	Circuit board mounting plate
MP21	01660-84501	1	Accessory pouch
MP22	01660-40502	1	Trim strip
MP23	01670-94302	1	ID label (HP 1670D)
MP23	01671-94302	1	ID label (HP 1671D)
MP23	01672-94302	1	ID label (HP 1672D)
MP24	01660-94302	1	Line switch label
MP25	01660-41901	1	Elastomeric keypad
MP26	01660-47401	1	RPG KNOB
MP27	01660-60002	1	Assembled keyboard panel and label
	01660-94303	0	Keyboard label-replacement
	01660-45201	0	Keyboard panel-replacement
MP29	01660-44703	1	Front panel spacer
MP30	01660-44702	1	Keyboard spacer
MP33	01670-04102	1	Probe cover plate (HP 1671D)
MP33	01670-04101	1	Probe cover plate (HP 1672D)
MP35	01660-94304		Label - pods and cable
MP36	0361-1272	4	Plastic Push Fastener (fan to rear panel)
MP37	1252-2218	2	20 pos. clip retainer (sweep cable)
MP38	1252-2220	1	34 pos. clip retainer (flexible disk drive to CPU board)
MP39	8160-0780	1	Ground Spring (acquisition board cable connectors)
W1	01650-61613	1	HP-IB cable
W2	01660-61613	1	Fan cable
W3	01660-61601	1	RS-232-C cable
W4	01660-61614	1	Flexible disk drive cable
W5	01660-61604	1	Cable - 60 Conductor
W6	01660-61607	1	Jumper cable assembly-orange
W7	01660-61608	1	Jumper cable assembly-wht
W8	54503-61606	1	Power supply cable
W10	01660-61609	1	Hard disk drive data cable
W11	01660-61610	1	Hard disk drive power cable
W12	01660-61611	1	I/O board cable
W13	01650-61601	1	Sweep cable (monitor assembly)
W14	16542-61607	1	Double probe adapter

HP 1670-Series Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
W15	8120-1521	1	Power cord - United States (7.5 ft)
W15	8120-1703	1	Power cord (Option 900-UK)
W15	8120-0696	1	Power cord (Option 901-Austl)
W15	8120-1692	1	Power cord (Option 902-Eur)
W15	8120-2296	1	Power cord (Option 906-Swit)
W15	8120-2957	1	Power cord (Option 912-Den)
W15	8120-4600	1	Power cord (Option 917-Africa)
W15	8120-4754	1	Power cord (Option 918-Japan)

Power Cables and Plug Configurations

This instrument is equipped with a three-wire power cable. The type of power cable plug shipped with the instrument depends on the country of destination. The W15 reference designators (table, previous page) show option numbers of available power cables and plug configurations.

8

Theory of Operation

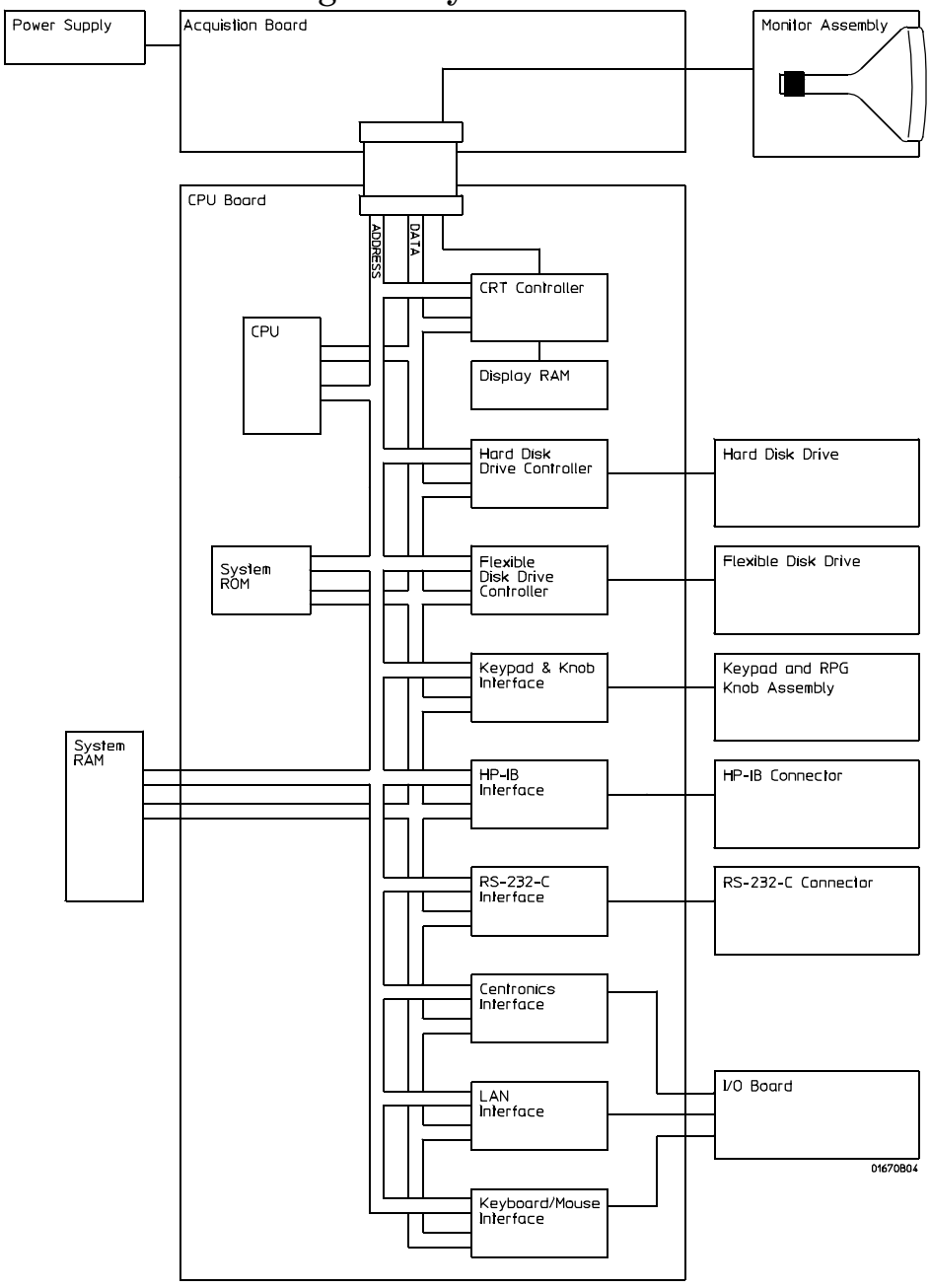
Theory of Operation

This chapter tells the theory of operation for the logic analyzer and describes the self-tests. The information in this chapter will help you understand how the logic analyzer operates and what the self-tests are testing. This information is not intended for component-level repair.

Block-Level Theory

The block-level theory is divided into two parts: theory for the logic analyzer and theory for the acquisition boards. A block diagram is shown with each theory.

The HP 1670D-Series Logic Analyzer



HP 1670D Logic Analyzer Block Diagram

HP 1670D Series Theory

CPU Board

The microprocessor is a Motorola 68EC020 running at 25 MHz. The microprocessor controls all of the functions of the logic analyzer including processing and storing data, displaying data, and configuring the acquisition ICs to obtain and store data.

System Memory

The system memory is made up of both read-only memory (ROM) and random access memory (RAM). Two types of ROM are used. A single 128Kx8 EPROM is used as a boot ROM, and four 512Kx8 flash ROMS are configured to provide a 256Kx32 flash ROM space. One 1Mx4byte SIMM provides 8MB RAM space.

On power-up, instructions in the boot ROM command the instrument to execute its boot routine. The boot routine includes power-up operation verification of the instrument subsystems and entering the operating system. The CPU searches for the operating system on flash ROM. Then, if the operating system is in flash ROM, the instrument will be initialized with the default configuration and await front panel instructions from you. If the operating system is not in flash ROM, the CPU accesses the disk drive to see if the operating system is on the disk.

The DRAM stores the instrument configuration, acquired data to be processed, and any inverse assembler loaded in the instrument by the user.

CRT Controller and Display RAM

A Brooktree BT475 RAMDAC color palette and a National Semiconductor LM1882CM video frame generator control the CRT. One of the RGB outputs of the color palette provides the eight-shade grey scale display. The video frame generator provides the horizontal and vertical synchronization timing signals.

The display RAM is a 256Kx8 video RAM and stores all of the pixel information used by the color palette. A serial address counter and an address multiplexer control the DRAM addressing. At the conclusion of each video frame the vertical sync signal from the video generator resets the serial address counter and a new frame is generated.

Disk Drive Controller

The disk drive controller consists of a single floppy drive controller IC. The floppy drive controller provides all signals to the disk drive including read and write data, read and write signals, write gate, and step signal. The floppy drive controller also reads status signals from the disk drive, including a track 00 signal, disk ready, and disk change signal.

Keypad and Knob Interface

The front panel keypad is scanned directly from the microprocessor address bus during the video blanking cycle of the CRT. When a front panel key is pressed the associated address bits are fed to the data bus through the pressed key and read by the microprocessor.

The rotary pulse generator (RPG) knob has its own interface circuit. Pulses and direction of rotation information are directed to the RPG interface. The microprocessor then reads and interprets the RPG signals and performs the desired tasks.

HP-IB Interface

The instrument interfaces to HP-IB as defined by IEEE Standard 488.2. The interface consists of an HP-IB controller and two octal drivers/receivers. The microprocessor routes HP-IB data to the controller. The controller then buffers the 8-bit HP-IB data bits and generates the bus handshaking signals. The data and handshaking signals are then routed to the HP-IB bus through the octal line drivers/receivers. The drivers/receivers provide data and control signal transfer between the bus and controller.

RS-232-C Interface

The instrument RS-232-C interface is compatible with standard RS-232-C protocol. The interface consists of a controller, and drivers/receivers. The controller serializes parallel data from the microprocessor for transmission. At the same time the controller also receives serial data and converts the data to parallel data characters for the microprocessor.

The controller contains a baud rate generator that can be programmed from the logic analyzer front panel for one of eight baud rates. Other RS-232-C communications parameters can also be programmed from the logic analyzer front panel.

The drivers/receivers interface the instrument with data communications equipment. Slew rate control is provided on the ICs eliminating the need for external capacitors.

CRT Monitor Assembly

The CRT Monitor Assembly consists of a monochrome CRT and a monitor driver board. The monitor driver board provides the biasing and control signals for the CRT. Pixel information is stored in the display RAM on the CPU board and is routed to the monitor driver board through the acquisition board and the sweep cable.

Flexible Disk Drive

The disk drive assembly is a high density disk drive that formats double-sided, double-density or high-density disks in LIF or DOS format. A disk drive controller on the CPU board controls the disk drive. Signals are routed directly to the disk drive through the disk drive cable.

Power Supply

A low voltage power supply provides all dc voltages needed to operate the logic analyzer. The power supply also provides the +5 Vdc voltage to the probe cables to power logic analyzer accessories and preprocessors.

Unfiltered voltages of +12 V, -12 V, +5 V, -5.2 V, and +3.5 V are supplied to the acquisition board where they are filtered and distributed to the CPU board, CRT Monitor Assembly, and probe cables.

Centronics Interface

The interface to the Centronics port includes latches and buffers. The latches and buffers convert the logic analyzer backplane signals into parallel Centronics signals.

LAN Interface

The LAN Interface is primarily a single LAN integrated circuit with supporting components. Isolation circuitry for the LAN port is included on the I/O board.

Keyboard/Mouse Interface

An 82C42PC PS2 controller makes up the PS2 Keyboard/Mouse interface. The PS2 controller interfaces the logic analyzer backplane with the keyboard and/or mouse devices.

I/O Board

The Input/Output (I/O) Board primarily includes a Centronics port and two mini-DIN (PS2) ports for the base 1670D-series products. The I/O board also includes isolation circuitry for the LAN.

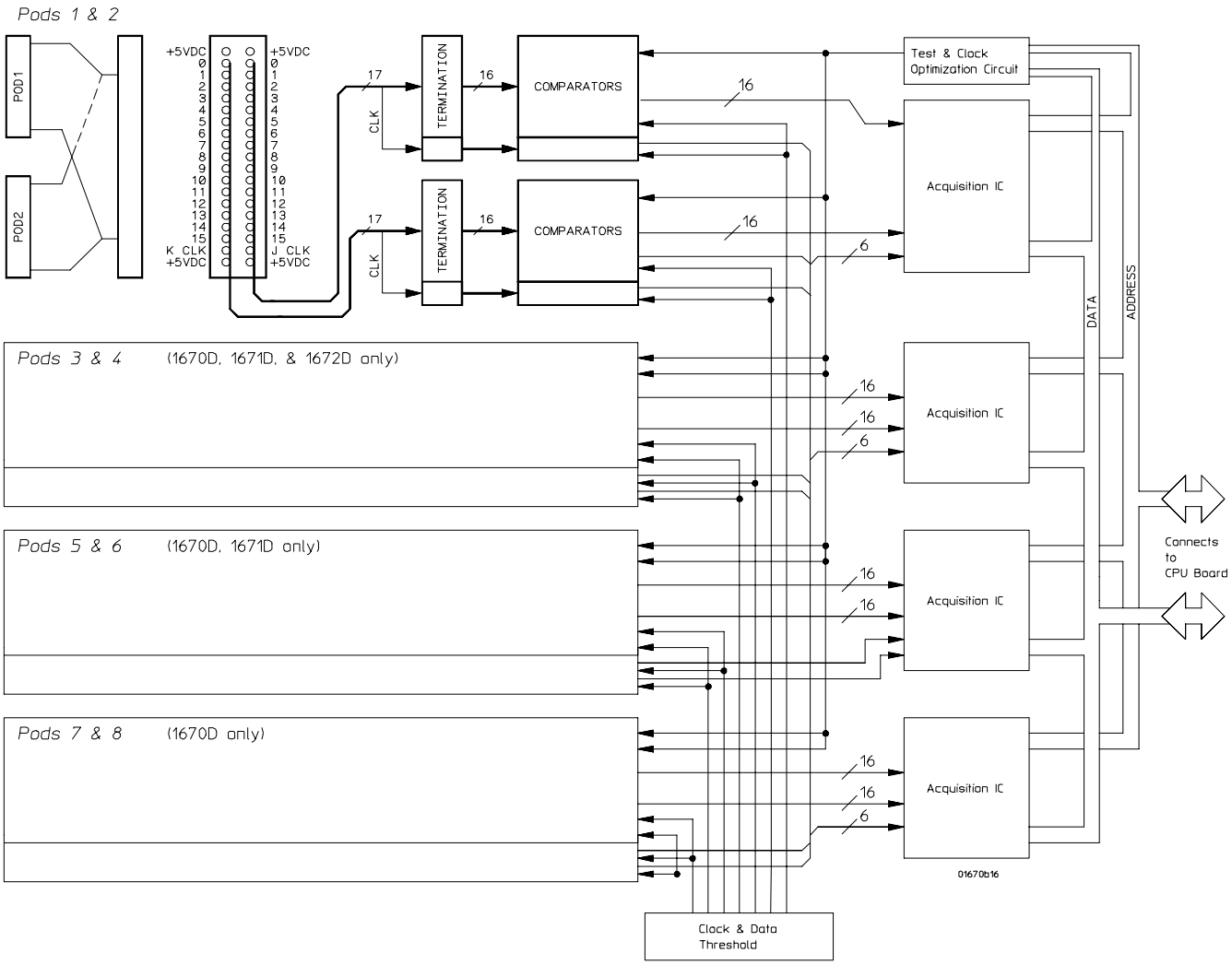
Hard Disk Drive Interface

Buffers interface the hard disk drive with the logic analyzer backplane.

Hard Disk Drive

The Hard Disk Drive is an IDE-compatible disk drive. A 40-pin IDE connector allows the disk drive to interface with the logic analyzer backplane through the hard disk drive interface.

The Logic Acquisition Board



Logic Acquisition Board Block Diagram

Logic Acquisition Board Theory

Probing

The probing circuit includes the probe cable and terminations. The probe cable consists of two 17-channel pods which are connected to the circuit board using a high-density connector. Sixteen single-ended data channels and one single-ended clock/data channel are passed to the circuit board per pod.

If the clock/data channel is not used as a state clock in state acquisition mode, it is available as a data channel. The clock/data channel is also available as a data channel in timing acquisition mode. Eight (HP 1670D), six (HP 1671D), or four (HP 1672D) clock/data channels are available as data channels, however only four clock/data channels can be assigned as clock channels in the HP 1670D and HP 1671D. All clock data channels available in the HP 1672D can be assigned as clock channels.

The cables use nichrome wire woven in polyarmid yarn for reliability and durability. The pods also include one ground path per channel in addition to a pod ground. The channel grounds are configured such that their electrical distance is the same as the electrical distance of the channel.

The probe tip assemblies and termination modules connected at the end of the probe cables have a divide-by-10 RC network that reduces the amplitude of the data signals as seen by the circuit board. This adds flexibility to the types of signals the circuit board can read in addition to improving signal integrity.

The terminations on the circuit board are resistive terminations that reduce transmission line effects on the cable. The terminations also improve signal integrity to the comparators by matching the impedance of the probe cable channels with the impedance of the signal paths of the circuit board. All 17 channels of each pod are terminated in the same way. The signals are reduced by a factor of 10.

Comparators

Two proprietary 9-channel comparators per pod interpret the incoming data and clock signals as either high or low depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparator ICs has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparator. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, all data and clock channel pipelines on the circuit board can be tested by the operating system software from the comparator.

Acquisition

The acquisition circuit is made up of a single HP proprietary ASIC. Each ASIC is a 34-channel state/timing analyzer, and one such ASIC is included for every two logic analyzer pods. All of the sequencing, pattern/range recognition, and event counting functions are performed on board the IC.

In addition to the storage qualification and counting functions, the acquisition ASICs also perform master clocking functions. All four state acquisition clocks are fed to each IC, and the ICs generate their own sample clocks. Every time you select RUN, the ICs individually perform a clock optimization before data is stored.

Clock optimization involves using programmable delays on board the IC to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase, 125-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (125 MHz and faster), the sample period is determined by the four-phase, 125-MHz clock signal.

For slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The sample clock is then fed to all acquisition ICs.

Threshold

A precision octal DAC and precision op amp drivers make up the threshold circuit. Each of the eight channels of the DAC is individually programmable which allows you to set the thresholds of the individual pods. The 16 data channels and the clock channel of each pod are all set to the same threshold voltage.

Test and Clock Synchronization Circuit

ECLinPS ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification. The test patterns are propagated across all data and clock channels and read by the acquisition ASIC to ensure both the data and clock pipelines are operating correctly.

The Test and Clock Synchronization Circuit also generates a four-phase, 125-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. The synchronizing signal keeps the internal clocking of the individual acquisition ASICs locked in step with the other ASICs at fast sample rates. At slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by all acquisition ICs.

Self-Tests Descriptions

The self-tests identify the correct operation of major functional areas in the logic analyzer. The self-tests are not intended for component-level diagnostics.

Three types of tests are performed on the HP 1670D-series logic analyzers: the power-up self-tests, the functional performance verification self-tests, and the parametric performance verification tests.

The power-up self-tests are performed when power is applied to the instrument.

The functional performance verification self-tests are run using a separate operating system, the performance verification (PV) operating system. The PV operating system resides on a separate disk that must be inserted in the disk drive when running the functional performance verification self-tests. The system and analyzer tests are functional performance verification tests.

Parametric performance verification requires the use of external test equipment that generates and monitors test data for the logic analyzer to read. The performance verification procedures in chapter 3 of this service guide make up the parametric performance verification for the logic analyzer. Refer to chapter 3, "Testing Performance," for further information about parametric performance verification.

Power-up Self-Tests

The power-up self-tests are divided into two parts. The first part is the system memory tests and the second part is the microprocessor interrupt test. The system memory tests are performed before the logic analyzer actually displays the power-up self-test screen. Both the system ROM and RAM are tested during power-up. The interrupt test is performed after the power-up self-test screen is displayed.

The following describes the power-up self-tests:

ROM Test

The ROM test performs several checksum tests on various read only memory elements, including the system ROM as well as the various software modules present in flash ROM.

Passing the ROM test implies that the microprocessor can access each ROM memory address and that each ROM segment provides checksums that match previously calculated values.

RAM Test

The RAM test checks the video RAM (VRAM), system dynamic RAM (DRAM), and static RAM memory within the real time clock IC. The microprocessor first performs a write/read in each memory location of the VRAM. At each VRAM memory location a test pattern is written, read, and compared. An inverse test pattern is then written, read, and compared. After verifying correct operation of the VRAM, the System RAM and real time clock RAM are tested in a similar fashion.

Passing the RAM test implies that the microprocessor can access each VRAM memory location and that each VRAM memory location can store a logical "1" or a logical "0." If the VRAM is functioning properly, the logic analyzer can construct a correct, undistorted display. Passing the RAM test also implies that the memory locations of system RAM can be accessed by the microprocessor and the data in RAM is intact, and that the memory locations inside the real time clock IC can store a logical "1" or a logical "0."

Interrupt Test

The Interrupt Test checks the microprocessor interrupt circuitry. With all interrupts disabled from their source, the microprocessor waits for a short period of time to see if any of the interrupt lines are asserted. An asserted interrupt line during the wait period signifies incorrect functioning of the device generating the interrupt or the interrupt circuitry itself. Those interrupts that can be asserted under software control are exercised to verify functionality.

Passing the Interrupt Test implies that the interrupt circuitry is functioning properly. Passing the Interrupt Test also implies that the interrupt generating devices are also functioning properly and not generating false interrupts. This means that the microprocessor can execute the operating system code and properly service interrupts generated by pressing a front panel key or receiving an HP-IB or RS-232-C command.

System Tests (SysPV)

The system tests are functional performance verification tests. The following describes the system tests:

ROM Test

The ROM test performs several checksum tests on various read only memory elements, including the system ROM as well as the various software modules present in flash ROM.

Passing the ROM test implies that the microprocessor can access each ROM memory address and that each ROM segment provides checksums that match previously calculated values.

RAM Test

The RAM test performs a write/read operation in each memory location in system dynamic RAM (DRAM). The video RAM in the display subsystem and the acquisition RAM in the data acquisition subsystem are not tested as part of the RAM test and are tested elsewhere. At each DRAM memory location, the code that resides at that location is stored in a microprocessor register. A test pattern is then stored at the memory location, read, and compared. An inverse test pattern is then stored, read, and compared. The original code is then restored to the memory location. This continues until all DRAM memory locations have been tested. The static RAM in the real time clock chip is also tested in a similar fashion.

Passing the RAM test implies that all RAM memory locations can be accessed by the microprocessor and that each memory location can store a logical "1" or a logical "0."

HP-IB Test

The HP-IB test performs a write/read operation to each of the registers of the HP-IB IC. A test pattern is written to each register in the HP-IB IC. The pattern is then read and compared with a known value.

Passing the HP-IB test implies that the read/write registers in the HP-IB IC can store a logical "1" or a logical "0," and that the HP-IB IC is functioning properly. Incoming and outgoing HP-IB information will not be corrupted by the HP-IB IC.

RS-232-C Test

This test checks the basic interface functions of the RS-232-C port. Both internal and external portions of the port circuitry are tested. In order for the RS-232-C test to pass, the RS-232-C loopback connector must be installed on the RS-232-C connector.

PS2 Test

The PS2 test exercises the PS2 interface between the logic analyzer and external keyboard, if an external keyboard is connected. First, a read/write operation is performed to each of the registers of the PS2 IC. A test pattern is written to each memory location, read, and compared with a known value. Second, if an external keyboard is connected to the PS2 port, the keyboard controller that resides in the keyboard is polled by the microprocessor. A test pattern is sent to the keyboard controller and returned to the microprocessor by the keyboard controller. The test pattern is then compared with a known value.

Passing the PS2 test implies that the read/write registers in the PS2 IC can store a logical "1" or a logical "0," and that the PS2 IC is functioning properly. Also, passing the PS2 test implies that the PS2 pathway to the external keyboard is functioning and that the keyboard controller can communicate with the microprocessor in the logic analyzer. Incoming PS2 information from the external keyboard will not be corrupted by the pathway between the keyboard controller and microprocessor.

Disk Test

The disk test verifies the operation of both the flexible disk drive and hard disk drive.

For the flexible disk drive, the disk test exercises the disk controller circuitry by performing a write/read on a disk. Either a LIF-formatted disk with 20 sectors available space or DOS-formatted disk with 5K available space is required and should be inserted in the disk drive. When the disk test is executed the disk is first checked sector by sector to find any bad sectors. If no bad sectors are found a test file will be created on the disk and test data will be written to the file. The file is then read and the test data compared with known values. The test file is then erased at the conclusion of the test.

For the hard disk drive, the disk test exercises the disk controller that is on the hard disk drive assembly. In addition, the buffers that make up the hard disk drive interface are tested. When the test is executed, the sectors of the hard disk are checked, and then write/read tested like the flexible disk drive.

Passing the disk test implies that the flexible disk controller circuitry in the logic analyzer and the disk read/write circuitry in the flexible disk drive are functioning properly. The flexible disk drive can read and write to a LIF- or DOS-formatted disk, and the data will not be corrupted by the flexible disk drive circuitry. Passing the disk test also imples that the hard disk drive controller circuitry, interface, and read/write circuitry are functioning properly, and that the data will not be corrupted by the hard disk drive circuitry.

Perform Test All

Selecting Perform Test All will initiate all of the previous functional verification tests in the order they are listed. The failure of any or all of the tests will be reported in the test menu field of each of the tests. The Perform All Test will not initiate the Front Panel Test or the Display Test.

Front Panel Test

A mock-up of the logic analyzer front panel is displayed on the CRT when the Front Panel Test is initiated. The operator then pushes each front panel button and turns the RPG (rotary pulse generator) knob to toggle the corresponding fields from light to dark on the front panel mock-up. Successively pushing any front panel key will cause the corresponding field to toggle back and forth between light and dark. An exception is the Done key. Pressing the Done key a second time will cause an exit of this test.

The Front Panel Test passes when all of the key fields in the front panel mock-up on the CRT can be toggled by pressing the corresponding front panel key, and the two RPG fields can be toggled by turning the knob. The Front Panel Test is not called when Perform Test All is selected.

Display Test

When initiated, the display test will cause three test screens to be displayed sequentially. The first test screen is a test pattern used to align the CRT. The other two screens verify correct operation of the greyscale palette by displaying first a full-bright screen and then a half-bright screen.

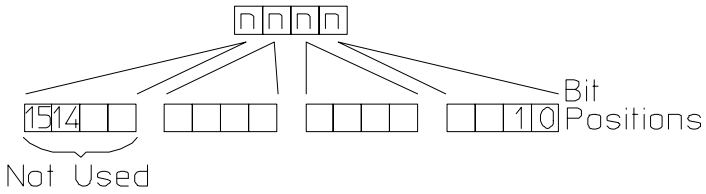
The pass or fail status of the display test is determined by the operator. The Display Test passes when all three test screens are displayed according to chapter 4, "Calibrating and Adjusting." The display test is not used when Perform Test All is selected.

LAN Test

The LAN test verifies the functionality of the LAN circuitry on the logic analyzer CPU board. A status code is returned for each of the LAN tests when each test is completed. The following figure shows the bit positions of the hexidecimal status reporting word.

A "1" in a bit position signifies that the bit is set and the test failed.

A "0" in a bit position signifies that the bit is not set and the test passed.



Status Reporting Message

Status Bits

Bit 0	The internal registers of the LAN IC are loaded with known test values and then are read. If this bit is not set, it implies that the LAN IC is operating properly and that the microprocessor can communicate with the LAN IC. If this bit is set, then the LAN module is not operational and must be replaced.
Bit 1	The CAM (Content Addressable Memory) bit reports whether the LAN address can be written from the LAN module Static RAM (SRAM) to the internal memory of the LAN IC. Also, the CAM bit reports whether the LAN address can be written to SRAM from the LAN IC. If this bit is not set, it implies that both the SRAM and the LAN IC internal memory are able to recognize and store the LAN address. If this bit is set, then the LAN module is not operational and must be replaced.
Bit 2	If this bit is not set, then the self-test has detected that the LAN cable is properly connected to the logic analyzer. If this bit is set, then the physical connection of the LAN cable must be checked.
Bit 3	If the Termination bit is set, then the self-test has detected an excessive number of collisions. The most probable cause of excessive collisions is an improperly terminated LAN cable. Provide a proper termination of the LAN cable according to the LAN topology being used.
Bit 4	The MAC (Media Access Control) bit indicates whether the Media Access Control unit on the LAN IC is functioning. If this bit is not set, it implies that both the transmit functions and receive functions of the LAN IC are operating properly. If this bit is set, then the LAN module is not able to properly transmit and receive packets and must be replaced.
Bit 5	The ENDEC (Encoder/Decoder) bit indicates whether the encoder/decoder internal to the LAN IC is functioning. The encoder/decoder is the interface between the MAC and the Ethernet transceiver. If this bit is set, then the ENDEC is not operating properly and the LAN module must be replaced.
Bit 6	The TRANS (Transceiver, such as Ethernet transceiver) bit indicates whether the circuitry between the LAN IC and the LAN cable is functioning. If this bit is not set, then the path between the LAN cable and the LAN IC is operating properly. If this bit is set, then either the CPU board or the I/O board must be replaced.
Bit 7	Timeout bit. If this bit is set, then bits 4, 5, or 6 will also be set. Refer to the appropriate bit for a suggested course of action.
Bit 8	The Tx bit indicates whether the transmission portion of the MAC, ENDEC, or TRANS test failed. Therefore, the Tx bit is used in conjunction with bits 4, 5, and 6. Refer to the appropriate bit for the suggested course of action.
Bit 9	The Rx bit indicates whether the receive portion of the MAC, ENDEC, or TRANS test failed. The Rx bit is used in conjunction with bits 4, 5, and 6. Refer to the appropriate bit for the suggested course of action.
Bit 10	The Parameters bit indicates the integrity of the LAN module self-test parameters. If this bit is not set, then the parameters sent to the self-test routine are correct. If this bit is set, then contact your nearest HP Sales and Service Office.
Bit 11	The EPROM that is used to hold the Ethernet address, IP address, and gateway address has been corrupted. If this bit is set, the LAN module must be replaced.
Bits 12–15	Not Used

Analyzer Tests (Analy PV)

The analyzer tests are functional performance verification tests. The self-tests identify the correct operation of major functional areas in the module. There are two sets of self-tests: the Board Verification Tests and the Acquisition IC Verification Tests. The self-tests are not intended for component-level diagnostics.

Board Verification Tests

The Board Verification Tests functionally verify the main subsystems of the module other than the acquisition ICs. Five tests are performed on the module subsystems. The tests are the PLD, Oscillator, Data Memory, Comparators, and Alignment Tests

PLD Test Programmable Logic Devices (PLD) are utilized as an interface between the acquisition board and the CPU board. The PLD Test verifies the operation of the data bus through the PLD. Test patterns are sent to the module and are written to a block of module memory. The patterns are then read and compared with known values. Also, a HW acceleration test verifies the PLD's high speed pattern search operation.

Passing the PLD Test implies that the PLD is not corrupted and that data can be passed between the acquisition board and the CPU board.

Oscillator Test The Oscillator Test functionally verifies the two oscillators and the oscillator internal pathways on the logic analyzer module. The oscillators are checked using the event counter on one of the acquisition ICs. The event counter will count the number of oscillator periods within a pre-determined time window. The count of oscillator periods is then compared with a known value.

Passing the Oscillator Test implies that both oscillators on the logic analyzer module are operating properly.

Data Memory Test After verifying the integrity of the memory address bus, the acquisition RAM is checked by filling the RAM with a checkerboard pattern of "1"s and "0"s then reading each memory location and comparing the test pattern with known values. Then the RAM is filled with an inverse checkerboard pattern, read, and compared with known values. The acquisition ICs are then used to generate a walking "1"s pattern, which is stored in RAM. The patterns are then read and compared with known values.

Passing the memory test implies that the acquisition RAM is functioning and that each memory location bit can hold either a logic "1" or logic "0." Passing this test also implies that the RAM is addressable by both the acquisition ICs and the mainframe CPU system through the CPU interface.

Alignment Test The alignment test exercises the clock optimization circuit on-board the acquisition IC. A test signal is generated by the comparators and sent to the acquisition IC. A test run is then done to see if the clock optimization circuit aligns the data signal with the master clock signal.

Passing the alignment test implies the clock optimization circuit that resides on the acquisition IC operates properly. Consequently the acquisition IC can properly sample data with minimal channel-to-channel skew.

Comparators Test The comparators in the logic analyzer front end are checked by varying the threshold voltage and reading the state of the activity indicators. The output of the comparator DAC is set to the upper voltage limit and the activity indicators for all the pod channels are read to see if they are all in a low state.

The DAC output is then set to the lower voltage limit, and the activity indicators are read to see if they are in a high state. The DAC output is then set to 0.0 V, allowing the comparators to recognize the test signal being routed to the test input pin of all of the comparators. Consequently, the activity indicators are read to see if they show activity on all channels of all the pods.

If the Comparators Test reveals that a logic analyzer channel is not recognizing the test data, a message will appear alerting the user that the channel is not operating as expected. If the module cannot be immediately serviced, then the user is alerted so that the failed channel is not used until the module can be serviced.

Passing the Comparators Test implies that the logic analyzer front end is operating properly and all channels are capable of passing data to the acquisition ICs.

Acquisition IC Verification Tests

During the Acquisition IC Verification Tests, five tests are performed on the acquisition ICs. The tests are the Communications, Encoder, Resource, Sequencer, and Clock Tests.

Communication Test The communication test verifies that communications pipeline between the various subsystems of the IC are operating. Checkerboard patterns of "1"s

and "0"s are routed to the address and data buses and to the read/write registers of each chip. After verifying the communications pipelines, the acquisition clock synchronization signals that are routed from IC to IC are checked. Finally, the IC master clock optimization path is checked and verified.

Passing the communication test implies that the communications pipelines running from subsystem to subsystem on the acquisition IC are functioning and that the clock optimization circuit on the IC is functioning. Also, passing this test implies that the acquisition clock synchronization signals are functioning and appear at the synchronization signal output pins of the acquisition IC.

Encoder Test The encoder is tested and verified using a walking "1" and walking "0" pattern. The walking "1" and "0" is used to stimulate all of the encoder output pins which connect directly to the memory ICs. Additionally, the post-store counter in each of the acquisition ICs is tested.

Passing the encoder test implies that the encoder is functioning and can properly route the acquired data to the acquisition memory. Also, passing this test implies that the post-store counter on the acquisition ICs is functioning.

Resource Test The pattern, range, edge, and glitch recognizers are tested and verified. First, an on-chip test register is verified for correct operation. Next, the pattern comparators are tested to ensure that each bit in the recognizer as well as the logic driver/receiver are operating. The edge and glitch pattern detectors are then verified in a similar manner. The range detectors are verified with their combinational logic to ensure that the in- and out-of-range conditions are recognized.

Passing the resource test implies that all of the pattern, range, edge, and glitch resources are operating and that an occurrence of the pattern, edge, or glitch of interest is recognized. Also, passing this test implies that the range recognizers will detect and report in- and out-of-range acquisition data to the sequencer or storage qualifier. The drivers and receivers at the recognizer input and output pins of the acquisition IC are also checked to be sure they are functioning.

Sequencer Test The sequencer, the state machine that controls acquisition storage, is tested by first verifying that all of the sequencer registers are operating. After the registers are checked, the combinational logic of the storage qualification is verified. Then, both the occurrence counter and the sequencer level counter is checked.

Passing the sequencer test implies that all 12 available sequence levels are functioning and that all possible sequence level jumps can occur. Also, passing this test implies that user-defined ANDing and ORing of storage qualified data patterns will occur, and that the occurrence counter that appears at each sequence level is functioning.

Chip Clock Test The sample clock generator on the acquisition ICs are tested by first checking the operation of the clock optimization circuit. The state acquisition clock paths are then checked to ensure that each state clock and clock qualifier are operating by themselves and in all possible clock and qualifier combinations. The timing acquisition optimization circuit is then operationally verified. Finally, the timing acquisition frequency divider (for slower timing sample rates) is checked.

Passing the chip clock test implies that each acquisition IC can generate its own master clock whether the clock is generated using a combination of external clocking signals (state mode) or internal sample clock signals (timing mode).

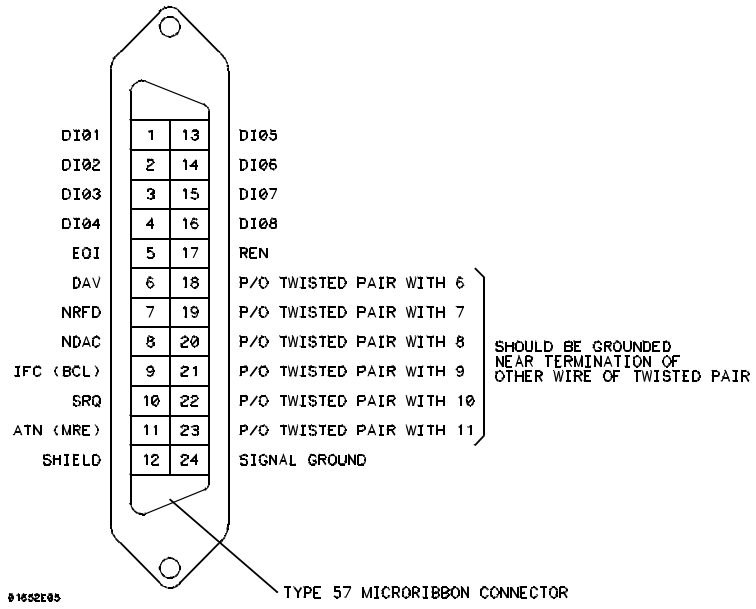
The Hewlett-Packard Interface bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programming Instrumentation." HP-IB is a carefully defined interface that simplifies the integration of various instruments and computers into systems. The interface makes it possible to transfer messages between two or more HP-IB compatible devices. HP-IB is a parallel bus of 16 active signal lines divided into three functional groups according to function.

Eight signal lines, called data lines, are in the first functional group. The data lines are used to transmit data in coded messages. These messages are used to program the instrument function, transfer measurement data, and coordinate instrument operation. Input and output of all messages, in bit parallel-byte serial form, are also transferred on the data lines. A 7-bit ASCII code normally represents each piece of data.

Data is transferred by means of an interlocking "Handshake" technique which permits data transfer (asynchronously) at the rate of the slowest active device used in that transfer. The data byte control lines coordinate the handshaking and form the second functional group.

The remaining five general interface management lines (third functional group) are used to manage the devices connected to the HP-IB. This includes activating all connected devices at once, clearing the interface, and other operations.

The following figure shows the connections to the HP-IB connector located on the rear panel.



HP-IB Interface Connector

The logic analyzer interfaces with RS-232-C communication lines through a standard 25-pin D connector. The logic analyzer is compatible with RS-232-C protocol. When a hardwire handshake method is used, the Data Terminal Ready (DTR) line, pin 20 on the connector, is used to signal if space is available for more data in the logical I/O buffer. Pin outs of the RS-232-C connectors are listed in the following table.

RS-232-C Signal Definitions

Pin Number	Function	RS-232-C Standard	Signal Direction and Level
1	Protective Ground	AA	Not applicable
2	Transmitted Data (TD)	BA	Data from Mainframe High = Space = "0" = +12 V Low = Mark = "1" = –12 V
3	Received Data (RD)	BB	Data to Mainframe High = Space = "0" = +3 V to +25 V Low = Mark = "1" = –3 V to –25 V
4	Request to Send (RTS)	CA	Signal from Mainframe High = ON = +12 V Low = OFF = –12 V
5	Clear to Send (CTS)	CB	Signal to Mainframe High = ON = +3 V to +12 V Low = OFF = –3 V to –25 V
6	Data Set Ready (DSR)	CC	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = –3 V to –25 V
7	Signal Ground	AB	Not applicable
8	Data Carrier Detect (DCD)	CF	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = –3 V to –25 V
20	Data Terminal Ready (DTR)	CD	Signal from Mainframe High = ON = +12 V Low = OFF = –12 V
23	Data Signal Rate Selector	CH/CI	Signal from Mainframe Always High = ON = +12 V

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This apparatus has been designed and tested in accordance with IEC Publication 348, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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About this edition

This is the first edition of the *HP 1670D-Series Logic Analyzers Service Guide.*

Publication number 01670-97006

Printed in USA.

Edition dates are as follows:

First edition, October 1996

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